MP18831

Isolated, Dual-Input Control, High-Side/Low-Side Half-Bridge Gate Driver

DESCRIPTION

The MP18831 is an isolated, half-bridge gate driver solution with up to 4A of source and sink peak current capability. The gate driver is designed to drive power switching devices with a short propagation delay and minimal pulse-width distortion. By utilizing MPS's proprietary capacitive-based isolation technology, the driver can provide up to $5kV_{RMS}$ withstand voltage (per UL 1577) (SOIC wide-body package option). It can also provide a common-mode transient immunity (CMTI) rating above 100kV/µs between the input side and output driver. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

The MP18831 integrates dual-channel gate drivers in one package. Each output can be grounded to the separated grounds, or connected to a positive or negative voltage reference. The secondary topology can be configured as a half-bridge high-side (HS) and low-side (LS) driver, which are each controlled by two independent input signals. To prevent shoot-through in the half-bridge driver, the MP18831 provides a configurable dead time (DT) set via an external resistor.

A wide primary-side VDDI supply voltage (V_{DDI}) range makes the driver suitable to be interfaced with 3.3V and 5V digital controllers. The secondary-side driver can accept up to a 30V supply. All of the supply voltage pins feature multiple under-voltage lockout (UVLO) protection options.

The MP18831 is available in SOIC-16 NB (narrow body), SOIC-16 WB (wide body), and LGA-13 (5mmx5mm) packages.

FEATURES

- Up to $5kV_{RMS}$ Input to Output Isolation (SOIC-16 WB Package)
- $1500V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (SOIC-16 NB and SOIC-16 WB Packages)
- $700V_{DC}$ Functional Isolation between Two Secondary-Side Drivers (LGA-13 Package)
- Common-Mode Transient Immunity (CMTI) >100kV/µs
- 2.8V to 5.5V Input VDDI Voltage (V_{DDI}) Range to Interface with TTL and CMOS-Compatible Inputs
- Up to 30V Output Drive Supply with Several Under-Voltage Lockout (UVLO) Options
- 4A Source, 4A Sink Peak Current Output
- 50ns Typical Propagation Delay
- Overlap Protection and Configurable Dead Time (DT) Control
- -40°C to +125°C Operating Temperature Range
- UL 1577 Certified:
  - SOIC-16 NB: $3kV_{RMS}$ Isolation for 60s
  - SOIC-16 WB: $5kV_{RMS}$ Isolation for 60s
  - LGA-13: $2.5kV_{RMS}$ Isolation for 60s
- DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Certified
  - SOIC-16 NB: $4242V_{PK}$ Isolation
  - SOIC-16 WB: $6000V_{PK}$ Isolation
  - LGA-13: $3535V_{PK}$ Isolation
- CQC Certification per GB 4943.1-2011
- Available in SOIC-16 NB, SOIC-16 WB, and LGA-13 (5mmx5mm) Packages

APPLICATIONS

- Half/Full-Bridge Converters
- Isolated DC/DC Converters
- Offline Isolated AC/DC Converters
- DC/AC Inverters

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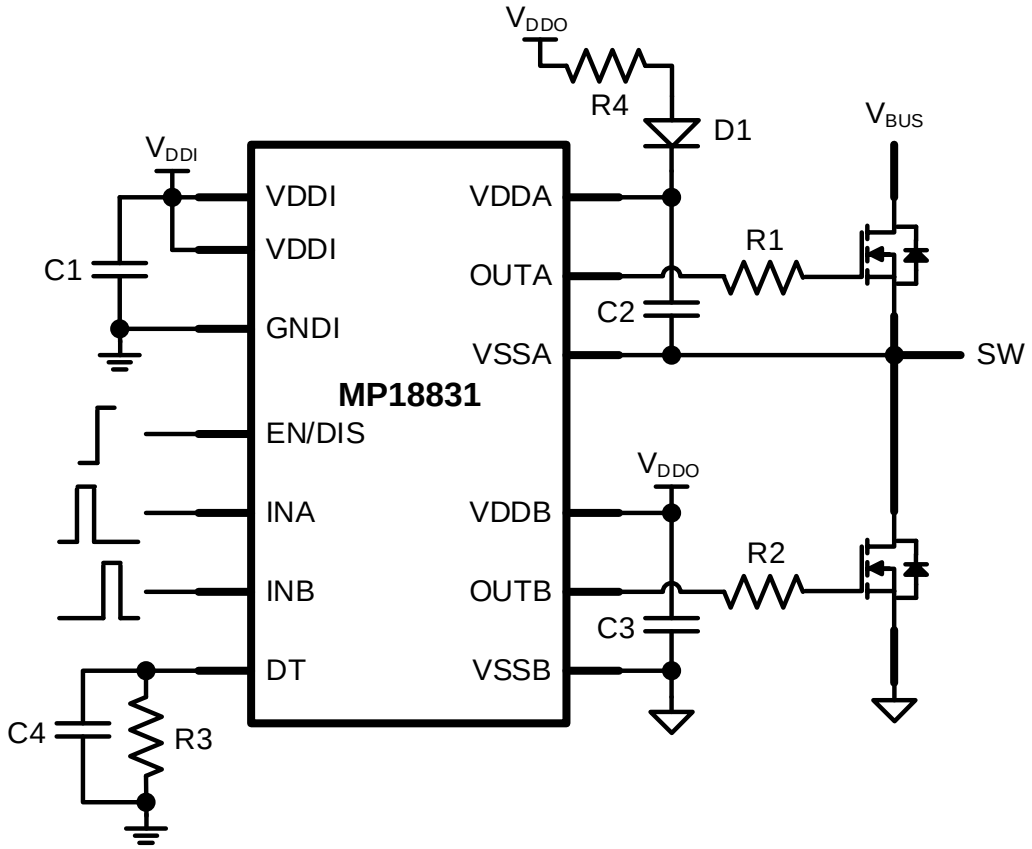
TYPICAL APPLICATION



SELECTION GUIDE

Part Number	Peak Output Current (A)	Output UVLO (V)	On/ Off Logic	Input Logic	Configuration	Overlap Protection	Config. Dead Time	Package
MP18831-4A	4	3	EN	INA/ INB	High-side (HS)/ low-side (LS) half-bridge	Yes	Yes	SOIC-16 NB, SOIC-16 WB, LGA-13 (5mmx5mm)
MP18831-4B		5						
MP18831-4C		8						
MP18831-4D		10						
MP18831-4E		12						
MP18831-A4A	4	3	DIS	INA/ INB	HS/LS half-bridge	Yes	Yes	SOIC-16 NB, SOIC-16 WB, LGA-13 (5mmx5mm)
MP18831-A4B		5						
MP18831-A4C		8						
MP18831-A4D		10						
MP18831-A4E		12						

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ORDERING INFORMATION (1)

Part Number*	Package	Top Marking	MSL Rating
MP18831-4AGSE	SOIC-16 NB	*See Below*	2
MP18831-4BGSE			
MP18831-4CGSE			
MP18831-4DGSE			
MP18831-4EGSE			
MP18831-A4AGSE			
MP18831-A4BGSE			
MP18831-A4CGSE			
MP18831-A4DGSE			
MP18831-A4EGSE			
MP18831-4AGY	SOIC-16 WB		3
MP18831-4BGY			
MP18831-4CGY			
MP18831-4DGY			
MP18831-4EGY			
MP18831-A4AGY			
MP18831-A4BGY			
MP18831-A4CGY			
MP18831-A4DGY			
MP18831-A4EGY			
MP18831-4AGLU	LGA-13 (5mmx5mm)		3
MP18831-4BGLU			
MP18831-4CGLU			
MP18831-4DGLU			
MP18831-4EGLU			
MP18831-A4AGLU			
MP18831-A4BGLU			
MP18831-A4CGLU			
MP18831-A4DGLU			
MP18831-A4EGLU			

* For Tape & Reel, add suffix -Z (e.g. MP18831-4AGSE-Z, MP18831-4AGY-Z, or MP18831-4AGLU-Z).

Note:

1) Contact MPS sales or our distributors to check the latest availability status for the ordering part numbers.

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TOP MARKING

MP18831-4X (SOIC-16 NB and SOIC-16 WB Packages)

MPS YYWW

M18831-4X

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
M18831-4X: Part number
X: UVLO level code, where X = A, B, C, D, or E
LLLLLLLLL: Lot number

TOP MARKING

MP18831-A4X (SOIC-16 NB and SOIC-16 WB Packages)

MPS YYWW

18831-A4X

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
18831-A4X: Part number
X: UVLO level code, where X = A, B, C, D, or E
LLLLLLLLL: Lot number

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TOP MARKING

MP18831-4X (LGA-13 5mmx5mm Package)

MPSYYWW

MP18831

LLLLLLL

4X

MPS: MPS prefix
YY: Year code
WW: Week code
MP18831: Part number
LLLLLLL: Lot number
4X: Remaining alphanumeric characters of part number
X: UVLO level code, where X = A, B, C, D, or E

TOP MARKING

MP18831-A4X (LGA-13 5mmx5mm Package)

MPSYYWW

MP18831

LLLLLLL

A4X

MPS: MPS prefix
YY: Year code
WW: Week code
MP18831: Part number
LLLLLLL: Lot number
A4X: Remaining alphanumeric characters of part number
X: UVLO level code, where X = A, B, C, D, or E

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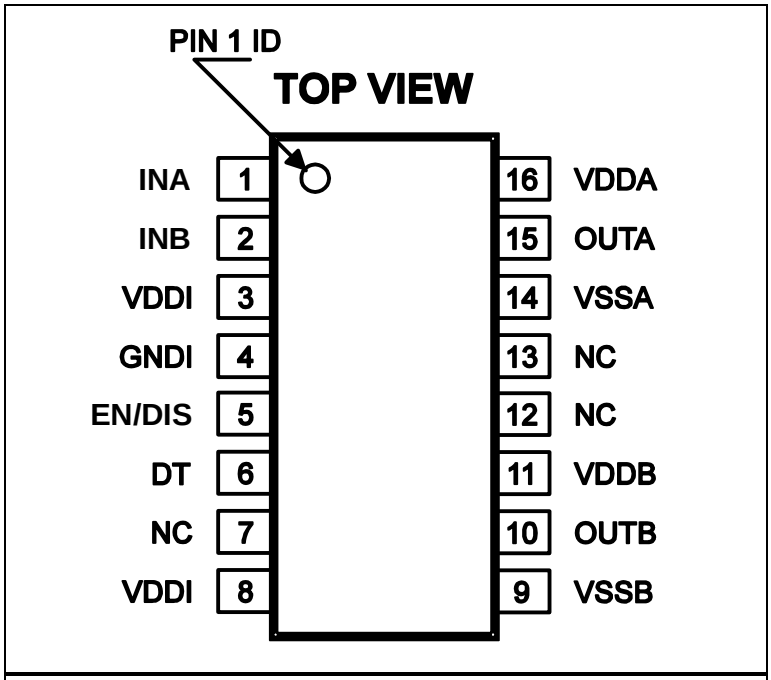
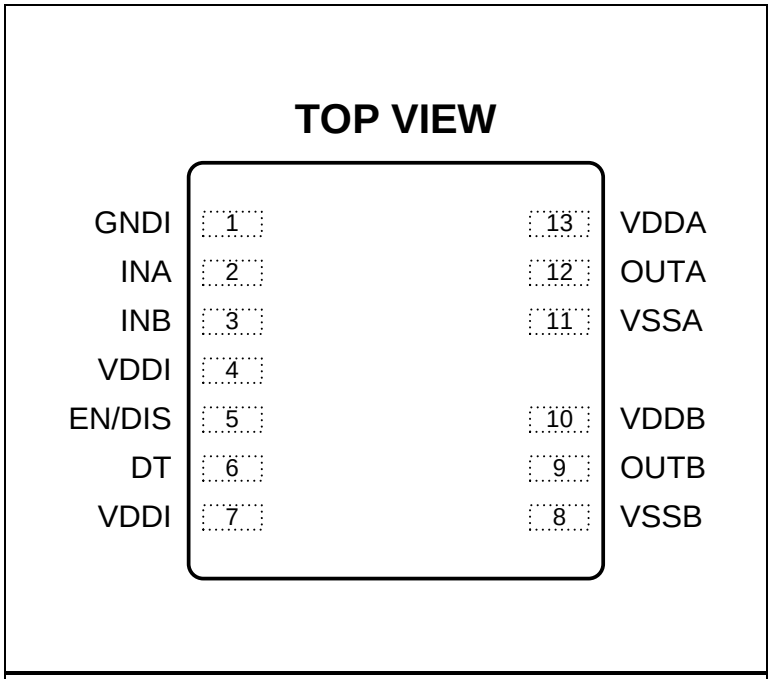
PACKAGE REFERENCE



SOIC-16 NB, SOIC-16 WB



LGA-13 (5mmx5mm)

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PIN FUNCTIONS

Pin #		Name	Description
SOIC-16 NB, SOIC-16 WB	LGA-13		
1	2	INA	**Non-inverting logic control signal input for driver A.** The INA pin can accept a TTL/CMOS level compatible input logic. This pin is internally pulled down to GNDI. It is recommended to tie this pin to GNDI if not used.
2	3	INB	**Non-inverting logic control signal input for driver B.** The INB pin can accept a TTL/CMOS level compatible input logic. This pin is internally pulled down to GNDI. It is recommended to tie this pin to GNDI if not used.
3, 8	4, 7	VDDI	**Input-side power supply input.** VDDI supplies power to the primary-side control circuitry. These two pins are internally shorted, and are locally decoupled to GNDI using a low-ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.
4	1	GNDI	**Input-side ground.** Reference ground for all input-side signals and internal control blocks.
5	5	EN	**Enable control input.** The EN pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. This pin is pulled high internally. Pull this pin high or leave it open to enable the chip; pull it low to shut down the driver output and disable the chip.
5	5	DIS	**Disable control input.** The DIS pin can be driven by an external TTL/CMOS level compatible input logic signal to enable/disable the chip. This pin is pulled low internally. Pull this chip low or leave it open to enable the chip; pull it high to shut down the driver output and disable the chip.
6	6	DT	**Dead time configuration input.** Leave the DT pin open to set the dead time to its minimum value. Tie a 2kΩ to 150kΩ resistor between DT and GNDI to set the dead time. It is recommended to place a 220pF or greater ceramic capacitor in parallel with this resistor for improved noise immunity.
7, 12, 13	-	NC	**Not connected.**
9	8	VSSB	**Output-side ground for driver B.** Reference ground for output driver B.
10	9	OUTB	**Gate drive output for driver B.** Connect this pin to the channel B power device gate.
11	10	VDDB	**Output-side driver power supply input for driver B.** This pin supplies power to the secondary-side driver B circuitry. It is locally decoupled to VSSB using a low-ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.
14	11	VSSA	**Output-side ground for driver A.** Reference ground for output driver A.
15	12	OUTA	**Gate drive output of driver A.** Connect this pin to the channel A power device gate.
16	13	VDDA	**Output-side driver power supply input for driver A.** This pin supplies power to the secondary-side driver A circuitry. It is locally decoupled to VSSA using a low-ESR/ESL bypass capacitor. The capacitor should be placed as close to the chip as possible.

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ABSOLUTE MAXIMUM RATINGS (2)

V_{DDI} - V_{GNDI} .....-0.3V to +6.5V
V_{INA}, V_{INB}, $V_{EN/DIS}$, V_{DT}
..... (V_{GNDI} - 0.3V) to (V_{DDI} + 0.3V)
V_{INA}, V_{INB}, $V_{EN/DIS}$ transient for 50ns
..... (V_{GNDI} - 5V) to (V_{DDI} + 0.3V)
V_{DDA} - V_{SSA}, V_{DDB} - V_{SSB} .....-0.3V to +35V
V_{OUTA} .....(V_{SSA} - 0.3V) to (V_{DDA} + 0.3V)
V_{OUTA} transient for 200ns
.....(V_{SSA} - 2V) to (V_{DDA} + 0.3V)
V_{OUTB} .....(V_{SSB} - 0.3V) to (V_{DDB} + 0.3V)
V_{OUTB} transient for 200ns
.....(V_{SSB} - 2V) to (V_{DDB} + 0.3V)
V_{SSA} - V_{SSB}
SOIC-16 NB, SOIC-16 WB ....-1500V to +1500V
LGA-13 (5mmx5mm) .....-700V to +700V
Continuous power dissipation (T_A = 25°C) (3)
SOIC-16 WB 2215mW
SOIC-16 NB 2115mW
LGA-13 (5mmx5mm) 1175mW
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 4000V
Charged device model (CDM) 2000V

Recommended Operating Conditions (4)

V_{DDI} - V_{GNDI} .....2.8V to 5.5V
V_{INA}, V_{INB}, $V_{EN/DIS}$ ..... V_{GNDI} to V_{DDI}
V_{DDA} - V_{SSA}, V_{DDB} - V_{SSB}
..... 4.2V to 30V (3V UVLO option)
..... 6.5V to 30V (5V UVLO option)
..... 9.2V to 30V (8V UVLO option)
..... 12V to 30V (10V UVLO option)
..... 14.5V to 30V (12V UVLO option)
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
SOIC-16 WB	56	30	°C/W
SOIC-16 NB	59	35	°C/W
LGA-13 (5mmx5mm)	106	50	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the MP18831 evaluation board, 2-layer PCB.

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ELECTRICAL CHARACTERISTICS

2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 5V/12V/15V [6], T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input-Side Supply Voltage						
V_{DDI} under-voltage lockout (UVLO) threshold	V_{DDI_UVLO}	(V_{DDI} - V_{GNDI}) falling	2.42	2.6	2.78	V
V_{DDI} UVLO hysteresis	$V_{DDI_UVLO_HYS}$		100	120	140	mV
Input-Side Supply Current						
VDDI shutdown current	I_{VDDI_SD}	V_{EN} = V_{GNDI} or V_{DIS} = V_{DDI}		1	1.3	mA
VDDI quiescent current	I_{VDDI_Q}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{GNDI}		1	1.3	mA
VDDI operating current	I_{VDDI}	f = 500kHz, 50% duty, C_{LOAD} = 100pF		2	2.8	mA
Logic Input (INA, INB, EN/DIS)						
Logic input high threshold	V_{LI_H}	(V_{LI} - V_{GNDI}) rising		1.6	1.8	V
Logic input low threshold	V_{LI_L}	(V_{LI} - V_{GNDI}) falling	1	1.2		V
Logic input hysteresis voltage	V_{LI_HYS}		360	400	440	mV
Internal pull-up resistance	R_{LI_PU}	EN		200		kΩ
Internal pull-down resistance	R_{LI_PD}	INA/INB, DIS		200		kΩ
Output-Side Supply Voltage						
V_{DDA}, V_{DDB} UVLO threshold when (V_{DDA} - VSSA) or (V_{DDB} - VSSB) is falling	V_{DDA_UVLO}, V_{DDB_UVLO}	-A, 3V threshold	2.7	3.2	3.7	V
		-B, 5V threshold	5	5.5	6	V
		-C, 8V threshold	7.5	8	8.5	V
		-D, 10V threshold	9.3	10	10.7	V
		-E, 12V threshold	11	12	13	V
V_{DDA}, V_{DDB} UVLO hysteresis	$V_{DDA_UVLO_HYS}$, $V_{DDB_UVLO_HYS}$	-A/-B, 3V/5V threshold	200	300	400	mV
		-C, 8V threshold	420	520	620	mV
		-D/-E, 10V/12V threshold	0.8	1	1.2	V
Output-Side Supply Current						
VDDA, VDDB shutdown current	I_{VDDA_SD}, I_{VDDB_SD}	V_{EN} = V_{GNDI} or V_{DIS} = V_{DDI}		1	1.3	mA
VDDA, VDDB quiescent current (current per channel)	I_{VDDA_Q}, I_{VDDB_Q}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{GNDI}		1	1.3	mA
VDDA, VDDB operating current (current per channel)	I_{VDDA}, I_{VDDB}	f = 500kHz, C_{LOAD} = 100pF, V_{DDA}/V_{DDB} = 12V		2.5	3	mA
		f = 500kHz, C_{LOAD} = 100pF, V_{DDA}/V_{DDB} = 15V		3	4.6	mA

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ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 5V/12V/15V [6], T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
Logic high output voltage	V_{OUTA_H}, V_{OUTB_H}	$I_{OUTA/OUTB}$ = -10mA	V_{DDA}/ V_{DDB} - 0.03	V_{DDA}/ V_{DDB} - 0.01		V
Logic low output voltage	V_{OUTA_L} V_{OUTB_L}	$I_{OUTA/OUTB}$ = 10mA		V_{SSA}/ V_{SSB} + 0.01	V_{SSA}/ V_{SSB} + 0.03	V
Peak output source current [7]	I_{OUTA_SRC}, I_{OUTB_SRC}	V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 15V, $V_{OUTA/OUTB}$ - $V_{SSA/SSB}$ = 5V (5V Miller plateau), f = 1kHz		-4		A
Peak output sink current [7]	I_{OUTA_SNK}, I_{OUTB_SNK}	V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 15V, $V_{OUTA/OUTB}$ - $V_{SSA/SSB}$ = 5V (5V Miller plateau), f = 1kHz		4		A
Output source resistance	R_{OUTA_H}, R_{OUTB_H}	$I_{OUTA/OUTB}$ = -10mA		1.3	2.5	Ω
Output sink resistance	R_{OUTA_L}, R_{OUTB_L}	$I_{OUTA/OUTB}$ = 10mA		1	2	Ω
Dead Time (DT) and Overlap Protection						
DT	t_{DT}	Leave DT open (minimum DT)		10	30	ns
		R_{DT} = 20kΩ	130	190	250	ns
		R_{DT} = 100kΩ	700	900	1100	ns
DT matching (|t_{DTAB} - t_{DTBA}|)	t_{DTM}			0	10	ns
Bias voltage for DT setting	V_{DT}	R_{DT} = 20kΩ	0.6	0.65	0.7	V
DT resistance range	R_{DT}		2		150	kΩ
Switching [8]						
Output rise time	t_R	($V_{OUTA/OUTB}$ - $V_{SSA/SSB}$) rising, C_{LOAD} = 1.8nF		10	20	ns
Output fall time	t_F	($V_{OUTA/OUTB}$ - $V_{SSA/SSB}$) falling, C_{LOAD} = 1.8nF		10	20	ns
Minimum pulse width	t_{PW_MIN}	Output pulse off if shorter than t_{PW_MIN}, C_{LOAD} = 0pF		23	35	ns
Propagation delay from INA/INB to the OUTA/OUTB rising edge	t_{PDLH}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, C_{LOAD} = 0pF	35	50	65	ns
Propagation delay from INA/INB to the OUTA/OUTB falling edge	t_{PDHL}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, C_{LOAD} = 0pF	35	50	65	ns

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ELECTRICAL CHARACTERISTICS *(continued)*

2.8V ≤ V_{DDI} - V_{GNDI} ≤ 5.5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 5V/12V/15V [6], T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Switching [8]						
Propagation delay from enable true to OUTA/OUTB rising edge	t_{PDEN}	$V_{INA/INB}$ = V_{DDI}, C_{LOAD} = 0pF	35	50	65	ns
Propagation delay from disable true to OUTA/OUTB falling edge	t_{PDDIS}	$V_{INA/INB}$ = V_{DDI}, C_{LOAD} = 0pF	35	50	65	ns
Pulse-width distortion $\lvert t_{PDLH} - t_{PDHL} \rvert$	t_{PWD}	C_{LOAD} = 0pF		1	6	ns
Propagation delay matching (channel-to-channel)	t_{PDM}	C_{LOAD} = 0pF		1	6	ns
Start-up delay from the input supply exiting UVLO to the output rising edge	t_{STU_VDDI}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{DDI}, C_{LOAD} = 0pF	15	25	35	μs
Shutdown delay from the input supply entering UVLO to the output falling edge [7]	t_{SHD_VDDI}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{DDI}, C_{LOAD} = 0pF		500		ns
Start-up delay from the output supply exiting UVLO to the output rising edge	t_{STU_VDDA}, t_{STU_VDDB}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{DDI}, C_{LOAD} = 0pF	10	20	30	μs
Shutdown delay from the output supply entering UVLO to the output falling edge [7]	t_{SHD_VDDA} t_{SHD_VDDB}	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{DDI}, C_{LOAD} = 0pF		500		ns
Static common-mode transient immunity (CMTI) [7]	$CMTI_{STC}$	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, $V_{INA/INB}$ = V_{GNDI} or V_{DDI}, slew rate of V_{GNDI} vs. $V_{SSA/SSB}$, V_{CM} = 1500V	100			kV/μs
Dynamic CMTI [7]	$CMTI_{DYN}$	V_{EN} = V_{DDI} or V_{DIS} = V_{GNDI}, f = 100kHz pulse at INA/INB, slew rate of V_{GNDI} vs. $V_{SSA/SSB}$, V_{CM} = 1500V	100			kV/μs

Notes:

6) For the test conditions, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 5V is used for 3V UVLO devices; V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V is used for 5V and 8V UVLO devices; and V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 15V is used for 10V and 12V UVLO devices.
7) Guaranteed by characterization, not production tested.
8) See Figure 1, Figure 2, and Figure 3 on page 19, as well as Figure 4, Figure 5, and Figure 6 on page 20 for details.

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INSULATION AND SAFETY-RELATED SPECIFICATIONS

Parameters	Symbol	Condition	SOIC-16 WB	SOIC-16 NB	LGA-13	Units
External air gap (clearance) (9)	CLR	Shortest pin-to-pin distance through the air between the primary and secondary sides	>8	>4	3.5	mm
External tracking (creepage) (9)	CPG	Shortest pin-to-pin distance across the package surface between the primary and secondary sides	>8	>4	3.5	mm
Distance through insulation	DTI	Internal clearance	>20	>20	>20	µm
Comparative tracking index	CTI	According to IEC60112	>600	>600	>600	V
Material group		According to IEC 60664-1	I	I	I	
Overvoltage category per IEC 60664-1		Rated mains voltages ≤ 150V_{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltages ≤ 300V_{RMS}	I-IV	I-III	I-III	
		Rated mains voltages ≤ 600V_{RMS}	I-III	I-II	-	
UL 1577, 5th Edition						
Recognized under UL 1577 Component Recognition Program, Single Protection. File number: E322138						
Dielectric withstand insulation voltage	V_{ISO}	V_{TEST} = V_{ISO} for t = 60s (qualification), V_{TEST} = 1.2 x V_{ISO} for t = 1s (100% production)	5000	3000	2500	V_{RMS}
DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 (10)						
Certified according to DIN EN IEC 60747-17 (VDE 0884-17): 2021-10; EN IEC 60747-17:2020+AC: 2021. Certification number: 40055265						
Maximum repetitive peak isolation voltage	V_{IORM}	AC voltage (bipolar)	891	560	560	V_{PK}
Maximum working isolation voltage	V_{IOWM}	AC voltage (sine wave)	630	400	400	V_{RMS}
		DC voltage	891	560	560	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM} for t = 6s (qualification), V_{TEST} = 1.2 x V_{IOTM} for t = 1s (100% production)	6000	4242	3535	V_{PK}
Apparent charge (11) measuring voltage	$V_{pd(m)}$	Method b1, at routine test (100% production), $V_{pd(ini)}$ = 1.2 x V_{IOTM}, t_{ini} = 1s, $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1s partial discharge < 5pC	1697	1061	1061	V_{PK}
Maximum surge isolation voltage (12)	V_{IOSM}	Tested per IEC 62368-1 with 1.2/50µs pulse, V_{TEST} = 1.3 x V_{IOSM} (qualification)	4000	4000	3500	V_{PK}
Barrier capacitance (13)	C_{IO}	f = 1MHz	~1	~1	~1	pF
Insulation resistance (13)	R_{IO}	V_{IO} = 500V, T_A = 25°C	>10^{12}			Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}			Ω
		V_{IO} = 500V, T_A = T_S = 150°C	>10^{9}			Ω
Pollution degree		Per DIN VDE 0110 Table 1	2			
Climatic category			40/125/21			

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INSULATION AND SAFETY-RELATED SPECIFICATIONS *(continued)*

GB 4943.1-2011
Certified according to CQC GB 4943.1-2011. File number: CQC22001348725, CQC22001348722, and CQC22001348723. SOIC-16 WB: Reinforced insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 700V_P maximum working voltage SOIC-16 NB: Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 660V_P maximum working voltage LGA-13: Basic insulation, altitude ≤ 5000m, 125°C thermal cycling test passed, 480V_P maximum working voltage

Notes:

9) See the Package Information on page 32 for detailed dimensions. As an isolated solution, the recommended land pattern is helpful to ensure adequate safety creepage and clearance distances on a PCB.
10) This coupler is suitable for "basic electrical insulation" only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
11) Electrical discharge caused by a partial discharge in the coupler.
12) The surge test is carried out in oil.
13) The barrier's primary-side and secondary-side terminals are connected, forming a two-terminal device. C_{IO} and R_{IO} are measured between the two terminals of the coupler.

SAFETY LIMITING VALUES (14)

Parameters	**Symbol**	**Condition**	**SOIC-16 WB**	**SOIC-16 NB**	**LGA-13**	**Units**
Maximum safety temperature (15)	T_S		150	150	150	°C
Maximum output safety current (current per channel)	I_{S_O}	V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V (16), T_J = 150°C, T_A = 25°C	91	87	48	mA
		V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 30V, T_J = 150°C, T_A = 25°C	36	35	19	mA
Safety power dissipation (17)	P_S	Input side	15	15	15	mW
		Output side, channel A	1100	1050	580	mW
		Output side, channel B	1100	1050	580	mW
		Total	2215	2115	1175	mW

Notes:

14) Maximum value allowed in the event of a failure.
15) The maximum safety temperature (T_S) has the same value as the maximum junction temperature, T_J (MAX), specified in the Absolute Maximum Ratings section on page 8.
16) Tested for 5V and 8V UVLO devices.
17) Test condition: V_{DDI} - V_{GNDI} = 5.5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 30V, T_J = 150°C, T_A = 25°C. The safety power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. This function can be calculated using the following equations:
$T_S = T_J (MAX) = T_A + (\theta_{JA} \times P_S)$
$P_S = I_S \times V_I$
Where V_I is the input voltage.

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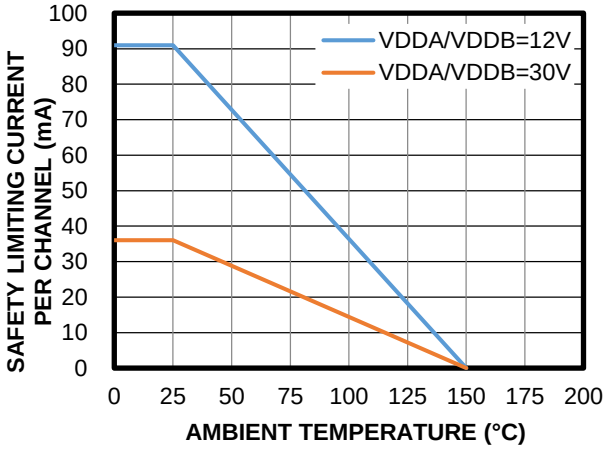
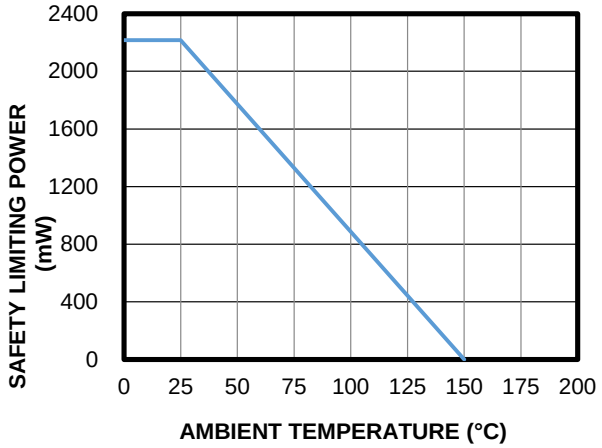
THERMAL DERATING CURVES FOR SAFETY LIMITING VALUES

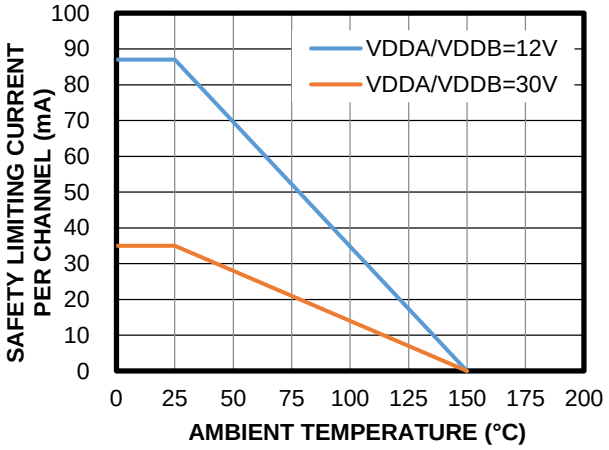
Thermal Derating Curve for Safety Limiting Current
SOIC-16 WB package



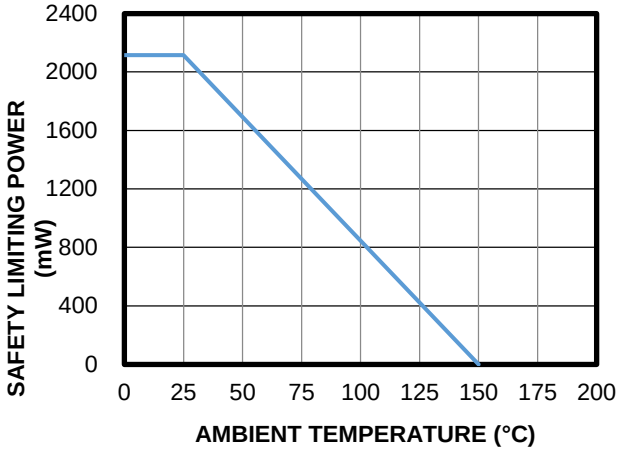
Thermal Derating Curve for Safety Limiting Power
SOIC-16 WB package



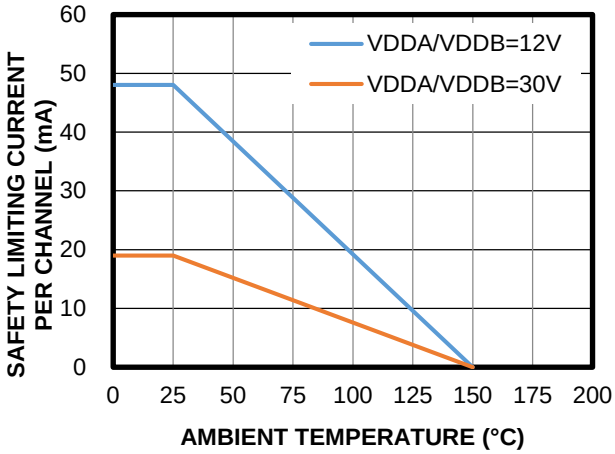
Thermal Derating Curve for Safety Limiting Current
SOIC-16 NB package



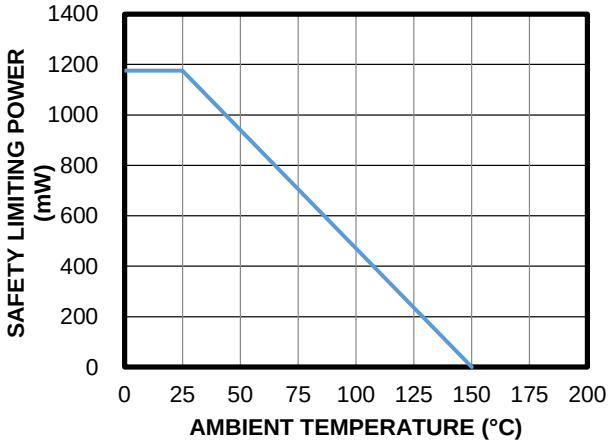
Thermal Derating Curve for Safety Limiting Power
SOIC-16 NB package



Thermal Derating Curve for Safety Limiting Current
LGA-13 package



Thermal Derating Curve for Safety Limiting Power
LGA-13 package



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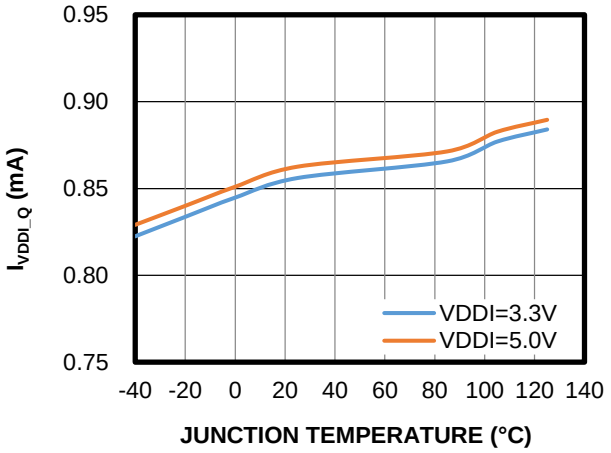
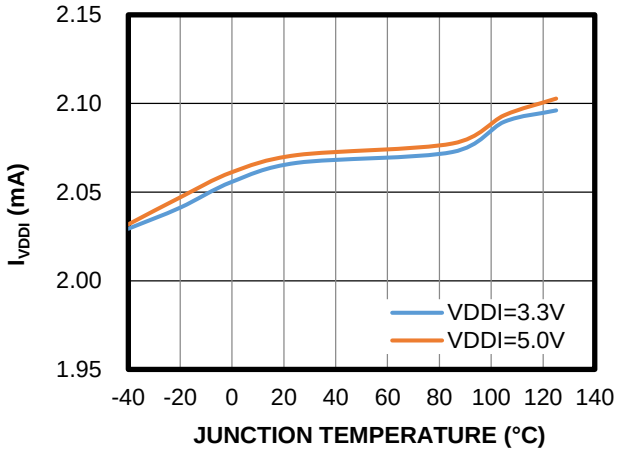
TYPICAL CHARACTERISTICS

V_{DDI} - V_{GNDI} = 5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

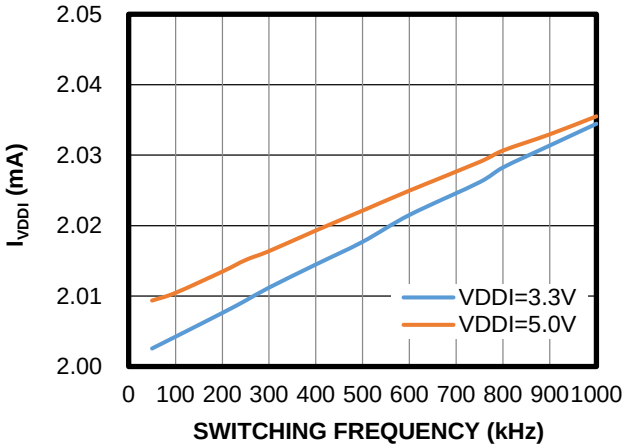
VDDI Quiescent Current vs. T_J
No switching



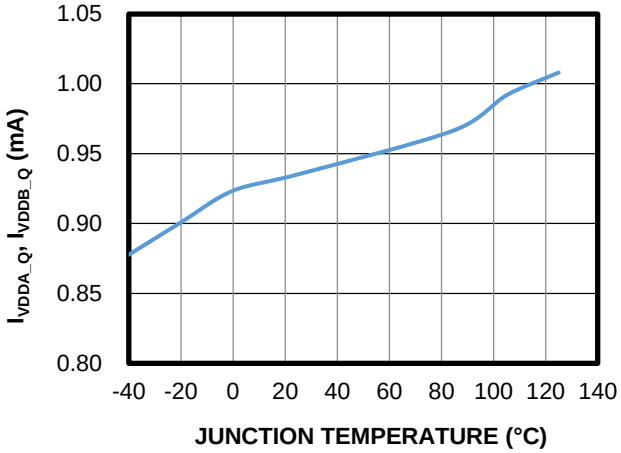
VDDI Operating Current vs. T_J
f = 500kHz, duty cycle = 50%



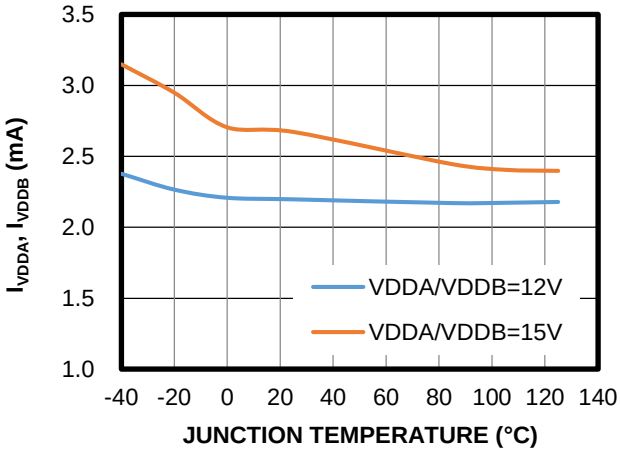
VDDI Operating Current vs. f_{SW}
Duty cycle = 50%



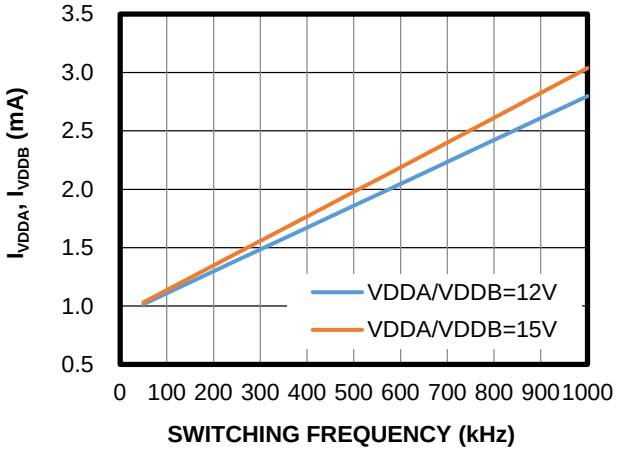
VDDA/VDDB Quiescent Current vs. T_J
Per channel, no switching



VDDA, VDDB Operating Current vs. T_J
Per channel, f = 500kHz, duty cycle = 50%, C_{LOAD} = 100pF



VDDA, VDDB Operating Current vs. f_{SW}
Per channel, duty cycle = 50%



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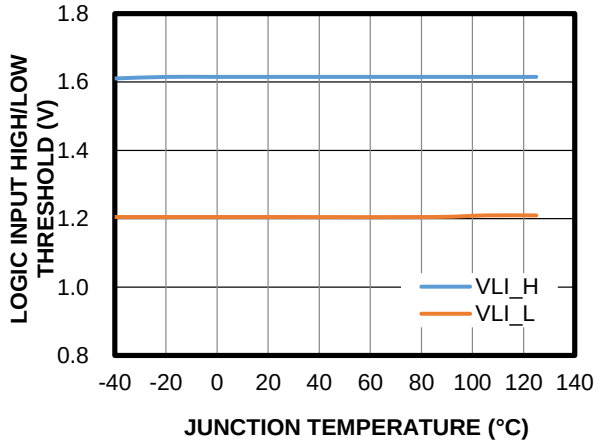
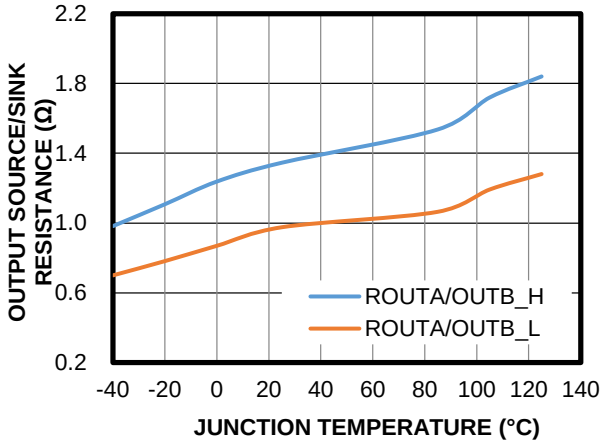
TYPICAL CHARACTERISTICS *(continued)*

V_{DDI} - V_{GNDI} = 5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

Logic Input High/Low Threshold vs. T_J

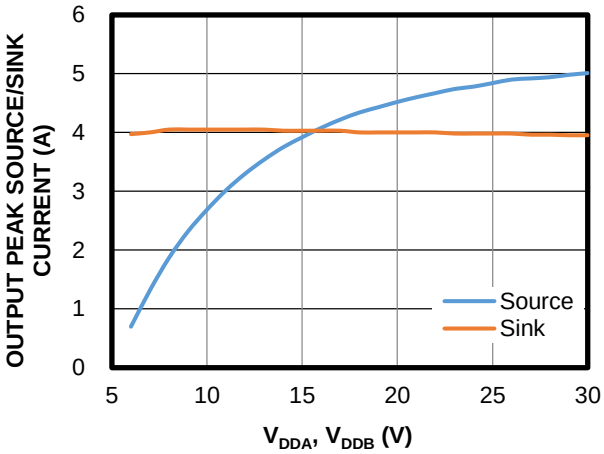


Output Source/Sink Resistance vs. T_J



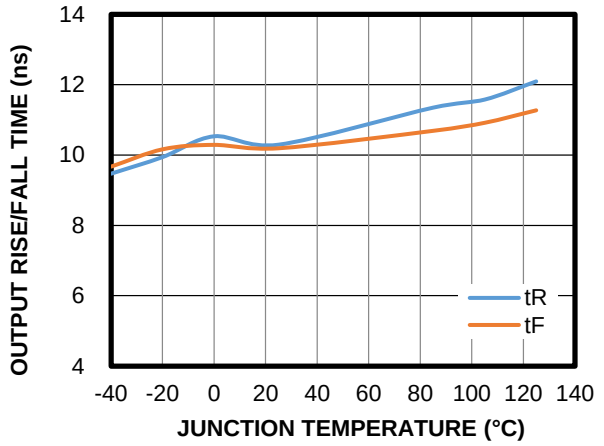
Output Peak Source/Sink Current vs. VDDA/VDDB Supply Voltage

5V UVLO version at 5V Miller plateau

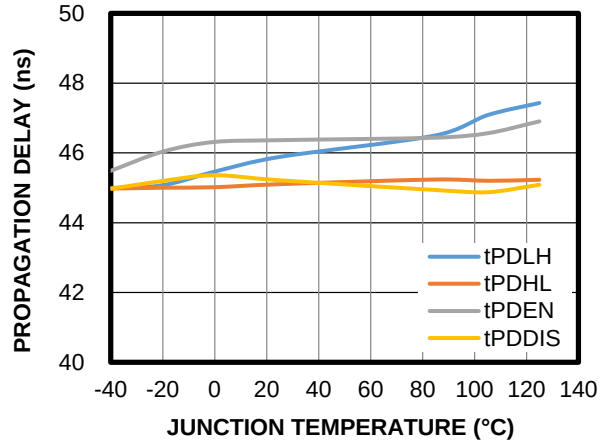


Output Rise/Fall Time vs. T_J

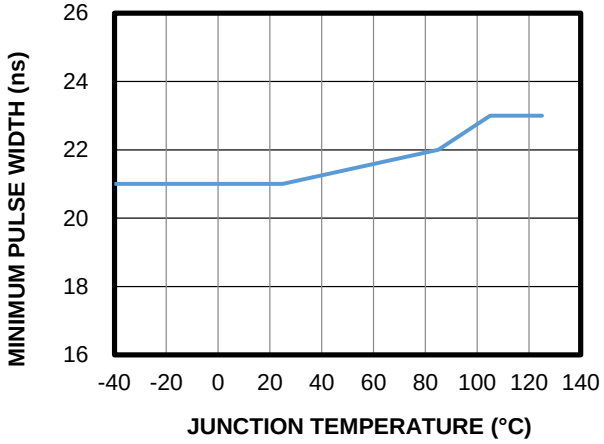
C_{LOAD} = 1.8nF



Propagation Delay vs. T_J



Minimum Pulse Width vs. T_J



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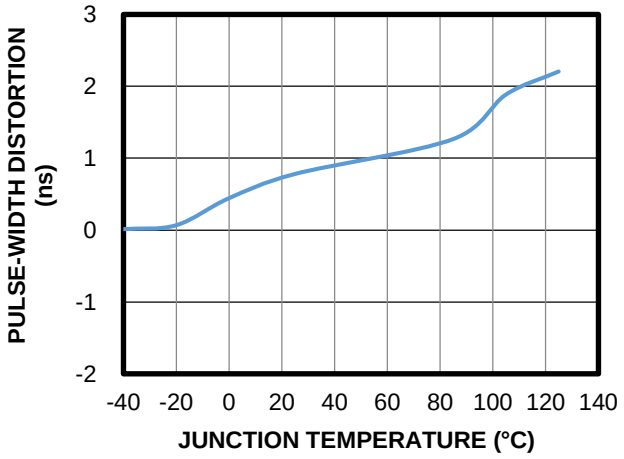
TYPICAL CHARACTERISTICS *(continued)*

V_{DDI} - V_{GNDI} = 5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V, C_{LOAD} = 0pF, T_J = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

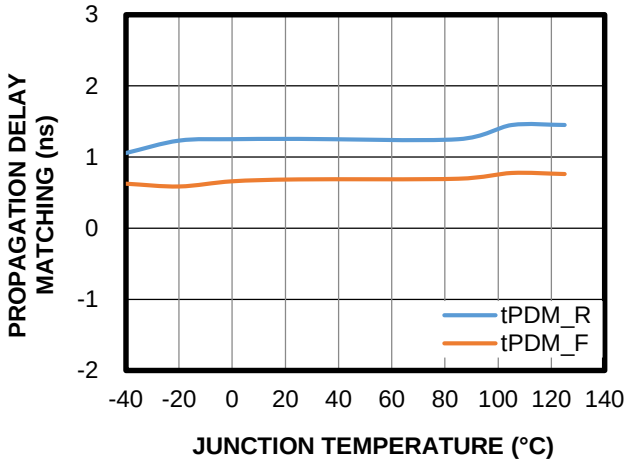
Pulse-Width Distortion vs. T_J

t_{PDLH} - t_{PDHL}

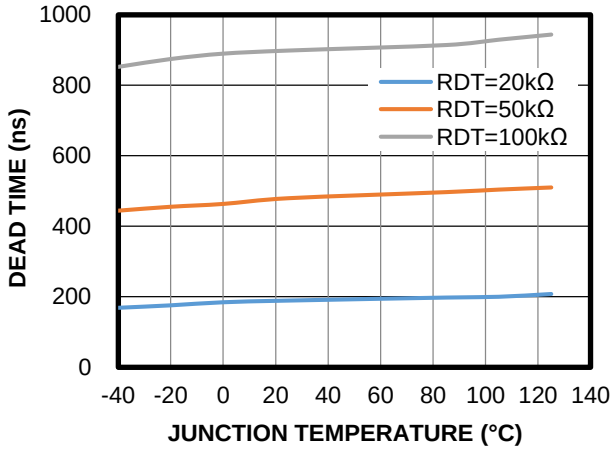


Propagation Delay Matching vs. T_J

t_{PDA} - t_{PDB}

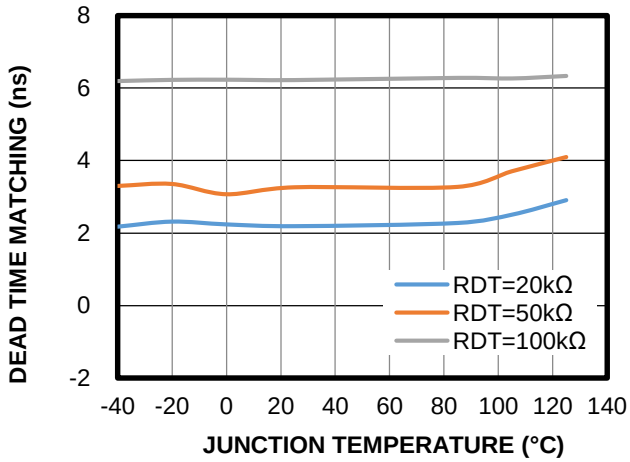


Dead Time vs. T_J



Dead Time Matching vs. T_J

t_{DTAB} - t_{DTBA}



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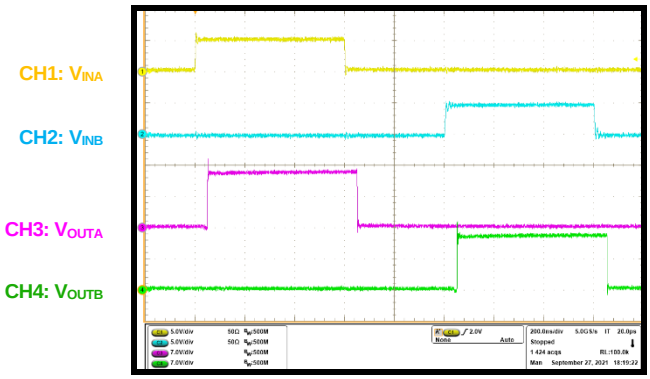
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{DDI} - V_{GNDI} = 5V, V_{DDA} - V_{SSA} = V_{DDB} - V_{SSB} = 12V, C_{LOAD} = 0pF, T_A = 25°C, all voltages with respect to the corresponding ground(s), unless otherwise noted.

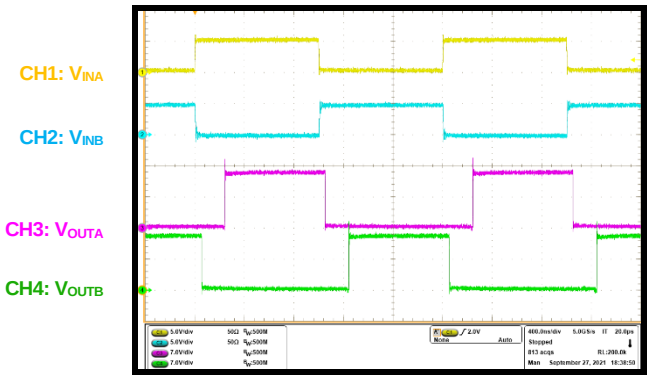
Typical Switching Waveforms

DT open



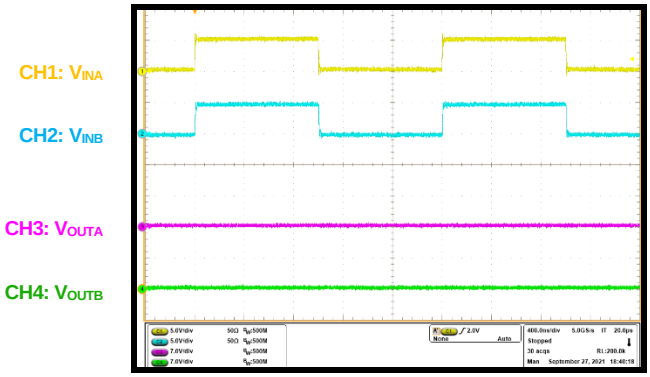
Dead-Time Control

R_{DT} = 20kΩ

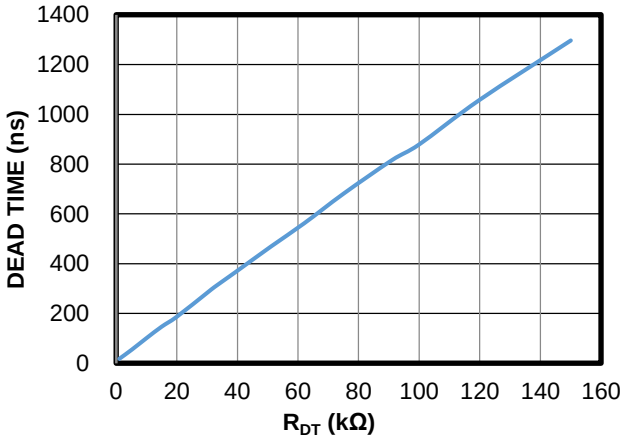


Overlap Protection

R_{DT} = 20kΩ



Dead Time vs. Dead Time Resistor



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DYNAMIC PARAMETERS DEFINITIONS

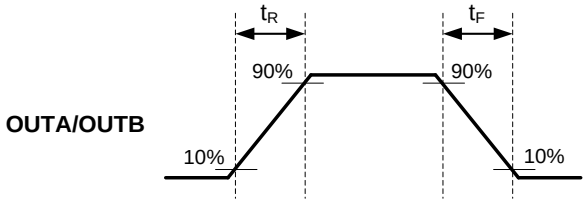

Figure 1: Output Rising and Falling Time

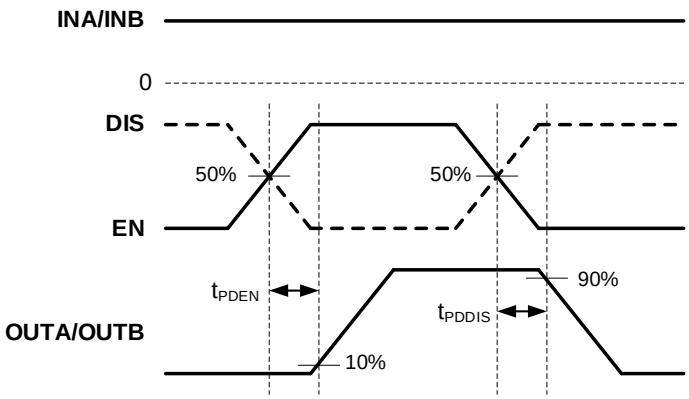

Figure 2: Enable/Disable Response Time

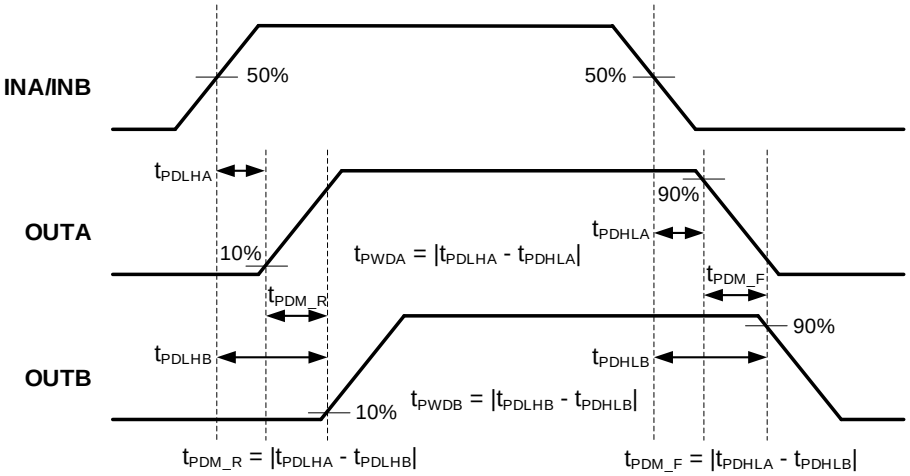

Figure 3: Propagation Delay Matching and Pulse-Width Distortion

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DYNAMIC PARAMETERS DEFINITIONS *(continued)*

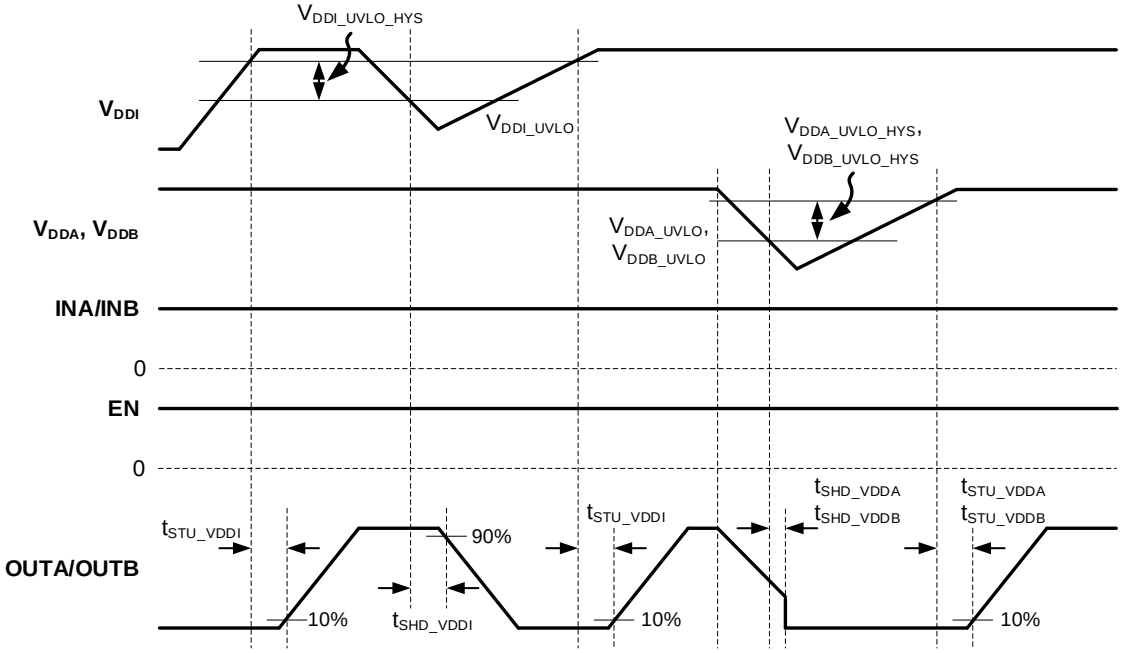

Figure 4: V_{DDI} and V_{DDA}, V_{DDB} Under-Voltage Lockout (UVLO)

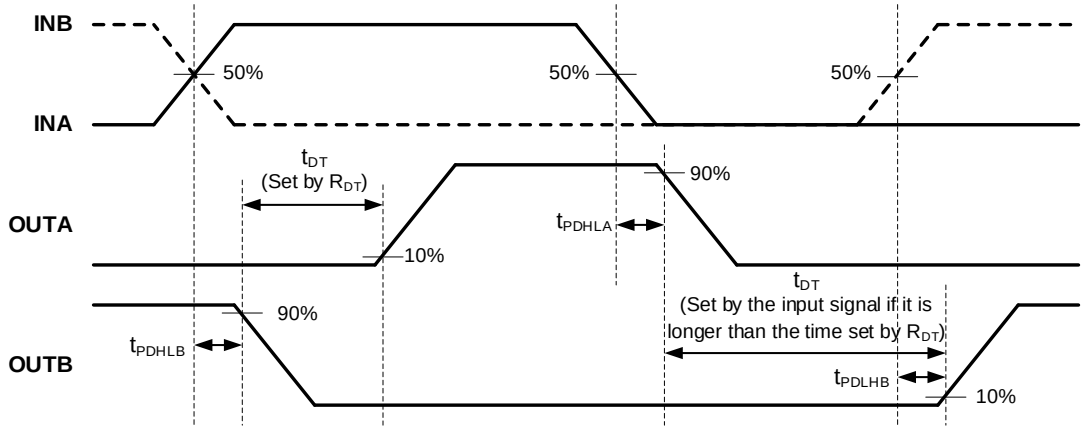

Figure 5: Dead Time Setting

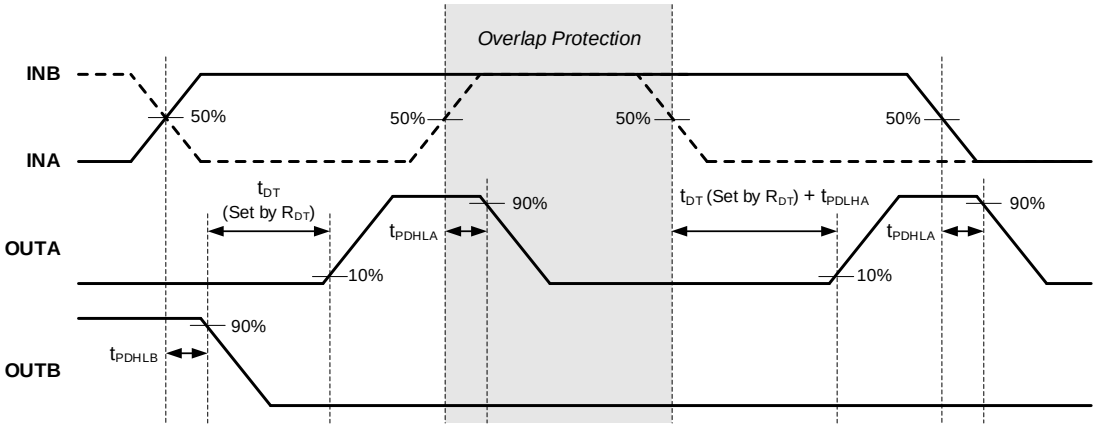

Figure 6: Overlap Protection and Recovery

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DEVICE FUNCTIONAL MODES

Table 1: Logic Truth Table (18) (19)

Inputs				Power Supply			Outputs		Notes
INA	**INB**	**EN**	**DIS**	**VDDI**	**VDDA**	**VDDB**	**OUTA**	**OUTB**	
L or O	L or O	H or O	L or O	P	P	P	L	L	Output transition occurs after DT expires
L or O	H	H or O	L or O	P	P	P	L	H	
H	L or O	H or O	L or O	P	P	P	H	L	
H	H	H or O	L or O	P	X	X	L	L	Invalid, overlap protection
X	X	L	H	P	X	X	L	L	The chip is disabled
X	X	X	X	UP	X	X	L	L	VDDI is unpowered
X	L or O	H or O	L or O	P	UP	P	L	L	VDDA is unpowered
L or O	H	H or O	L or O	P	UP	P	L	H	
L or O	X	H or O	L or O	P	P	UP	L	L	VDDB is unpowered
H	L or O	H or O	L or O	P	P	UP	H	L	

Notes:

18) L: Logic low; H: Logic high; O: Open; X: Not applicable; P: Powered; UP: Unpowered, UVLO condition.
19) If VDDI is powered, the output can operate functionally as long as this channel is powered normally.

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FUNCTIONAL BLOCK DIAGRAM

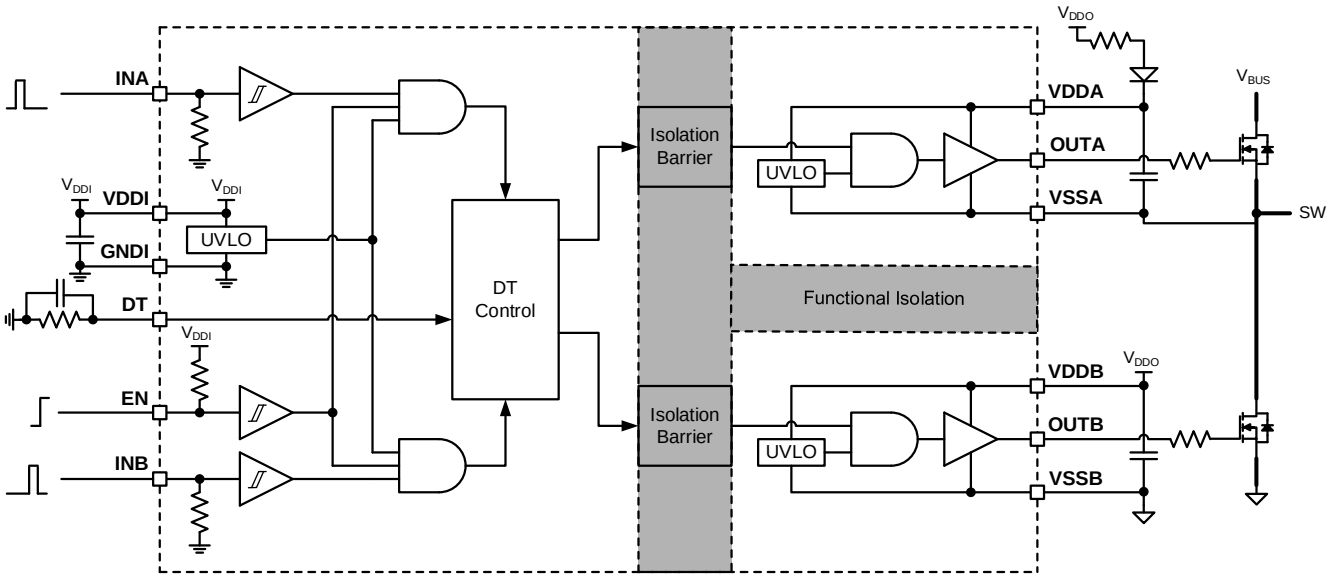

Figure 7: Functional Block Diagram (MP18831-4x, Enable Control Logic)

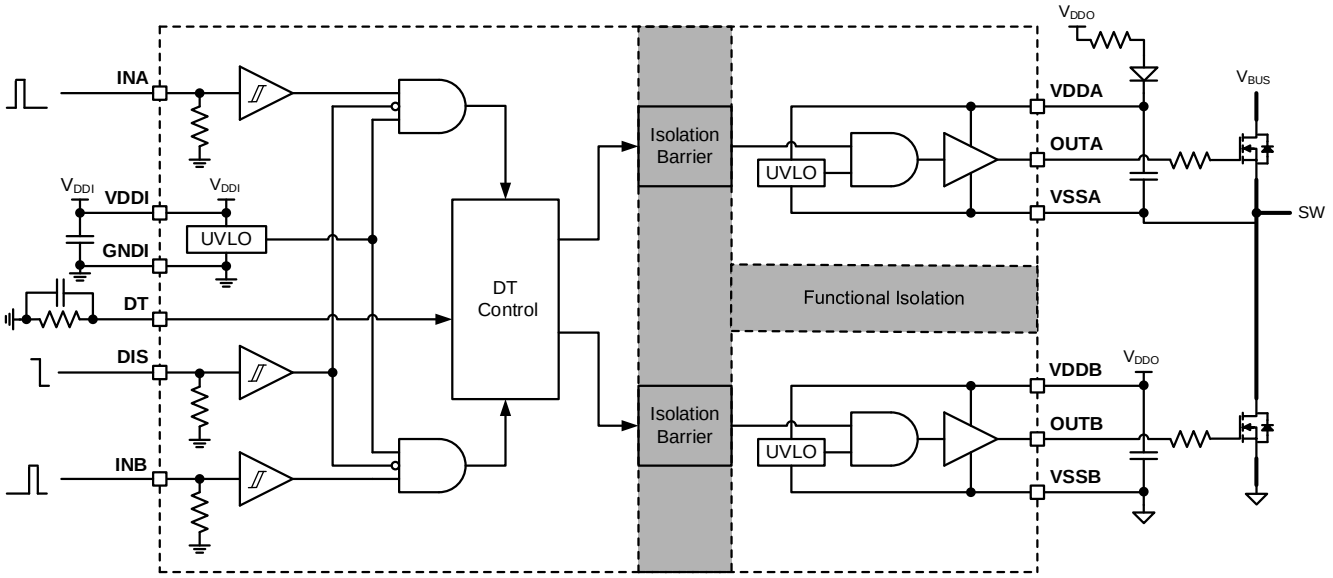

Figure 8: Functional Block Diagram (MP18831-A4x, Disable Control Logic)

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OPERATION

The MP18831 is an isolated, dual-input control, half-bridge gate driver solution with 4A peak output current capability. This IC is designed to drive power switching devices with a short propagation delay and minimal pulse-width distortion. These advanced features enable high efficiency, high power density, and robustness in a wide variety of power applications.

See Table 1 on page 22 for device functional modes.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to avoid the chip or certain blocks from operating at insufficient supply voltage. The MP18831 incorporates internal UVLO comparators for all of the input and output supply circuit blocks to monitor the VDDI, VDDA, and VDDB voltages (V_{DDI}, V_{DDA}, and V_{DDB}, respectively). Figure 4 shows the input and output supply UVLO time sequence diagram.

If the input bias voltage (V_{DDI}) is unpowered or under the UVLO threshold, the chip is not enabled and the output stages do not receive the control signals from the input stage. The UVLO mechanism holds the output forced low, regardless of the present logic levels of the input signals (including EN/DIS and INA/INB).

If either output stage of the driver is unpowered or below its UVLO threshold, the corresponding channel's output is also pulled low. As long as either channel is powered normally, the corresponding channel can accept the related control signal.

Input Stage and On/Off Control

All of the control input pins (EN/DIS and INA/INB) accept a TTL/CMOS compatible logic input that is reliably isolated from each output. These control pins can easily be driven with common logic-level signals from a digital controller. However, any input signal applied to these control pins must never exceed the input stage supply, V_{DDI}. Therefore, it is recommended to tie VDDI to the same power supply as the control signal sources. The control logic for EN, INA, and INB are active high, while the control logic for DIS is active low.

If the INA/INB inputs are left open, they are forced logic low via the internal pull-down resistors. This configuration ensures that the corresponding output remains low if the control input is not connected. If either logic input pin (INA or INB) is not being used, it is recommended to externally connect it to ground for better noise immunity and stable operation.

Similarly, for on/off control, the EN pin is tied to VDDI via the internal pull-up resistor, while the DIS pin is connected to GNDI via the internal pull-down resistor. Although leaving EN/DIS pin floating does allow the chip to operate normally after start-up, it is recommended to provide a stable external signal input for on/off control in actual applications.

Output Stage

The MP18831's output stage is comprised of an upper P-channel MOSFET and a lower N-channel MOSFET (see Figure 9). The effective output pull-up source resistance R_{OUTA_H}/R_{OUTB_H} is the on resistance of the upper P-channel MOSFET, which delivers the large peak source current during the external power switch turn-on transition. The pull-down structure is an N-channel MOSFET, for which the on resistance (R_{OUTA_L}/R_{OUTB_L}) is the output effective pull-down impedance when the device is driven low.

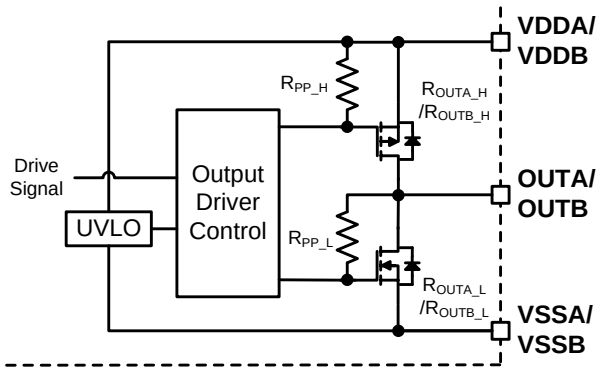

Figure 9: Output Stage

The output stage is optimized to provide strong driving capacity to a power device during the Miller plateau interval of the on/off switching procedure.

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The MP18831 is capable of delivering 4A peak source/sink current pulses. The rail-to-rail output ensures that the voltage switches between V_{DDA}/V_{DDB} and V_{SSA}/V_{SSB}, respectively.

Configurable Dead Time (DT) and Overlap Protection

To prevent the occurrence of shoot-through in the half-bridge driver, the MP18831 allows the user to adjust the dead time (DT), which inserts a user-configurable delay between the transitions of OUTA and OUTB. Generally, the MP18831 always selects operating DT to be the longer delay time between the driver's configured DT and the input control signals' DT.

When the DT control is enabled, the overlap protection scheme is also activated. If both control inputs are logic high synchronously, the outputs of both the channels are blocked and clamped low immediately. This overlap protection does not affect the DT setting of normal operation. The output low-clamping status remains until either input signal drops to logic low.

The DT delay operation is present on all output transitions from low to high, including normal switching and overlap protection recovery (see Figure 5 and Figure 6 on page 20 for more details about DT operation and the overlap protection mechanism).

The chip's DT is set via the DT pin. A steady-state bias voltage of about 0.65V is generated on the DT pin. The DT pin's source current is monitored to adjust the DT delay. If the DT pin is left open, a minimum DT (t_{DT}) is set. DT is typically configured by connecting a single resistor (R_{DT}) from the DT pin to the input stage ground, GNDI. R_{DT} should be between the 2kΩ and 150kΩ, and a filter capacitor in parallel of at least 220pF is recommended (see the Typical Performance Characteristics on page 18 for the Dead Time vs. R_{DT} curve).

Common-Mode Transient Immunity (CMTI)

Common-mode transient immunity (CMTI) is one of the key characteristics that determines an isolator's robustness, and is especially important in high-voltage applications that utilize devices with fast transient response (e.g. SiC/GaN FET). When a power device is switching, the high slew rate dv/dt or di/dt transient noise can corrupt the signal transmission across the isolation barrier (see Figure 10 and Figure 11).

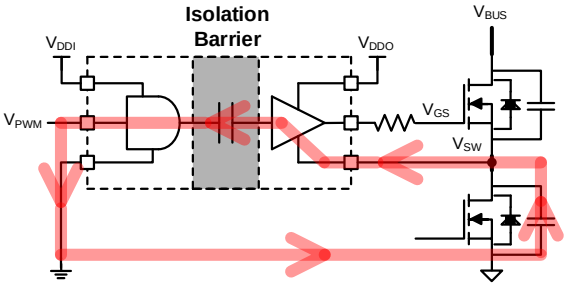

Figure 10: High Slew Rate Transient Noise Coupling Path

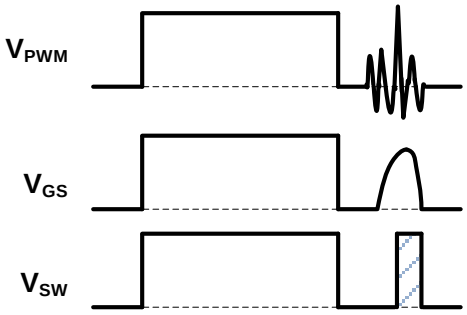

Figure 11: Abnormal Pulse Caused by Coupled Noise if dv/dt > CMTI

CMTI is defined as the maximum tolerable rate-of-rise (or fall) of a common-mode voltage applied between two isolated circuits, given in volts per second (V/ns or kV/µs). Below the maximum slew rate of a common-mode voltage, the isolator's output remains at the specified logic level and timing.

Figure 12 on page 26 shows the CMTI test set-up to measure the CMTI of a coupler in both static and dynamic operation, under the specified common-mode pulse magnitude (V_{CM}), the specified slew rate for the common-mode pulse (dV_{CM}/dt), and other specified test or ambient conditions. The isolator's output should remain in the correct state as long as the pulse magnitude and the slew rate meet the CMTI specifications.

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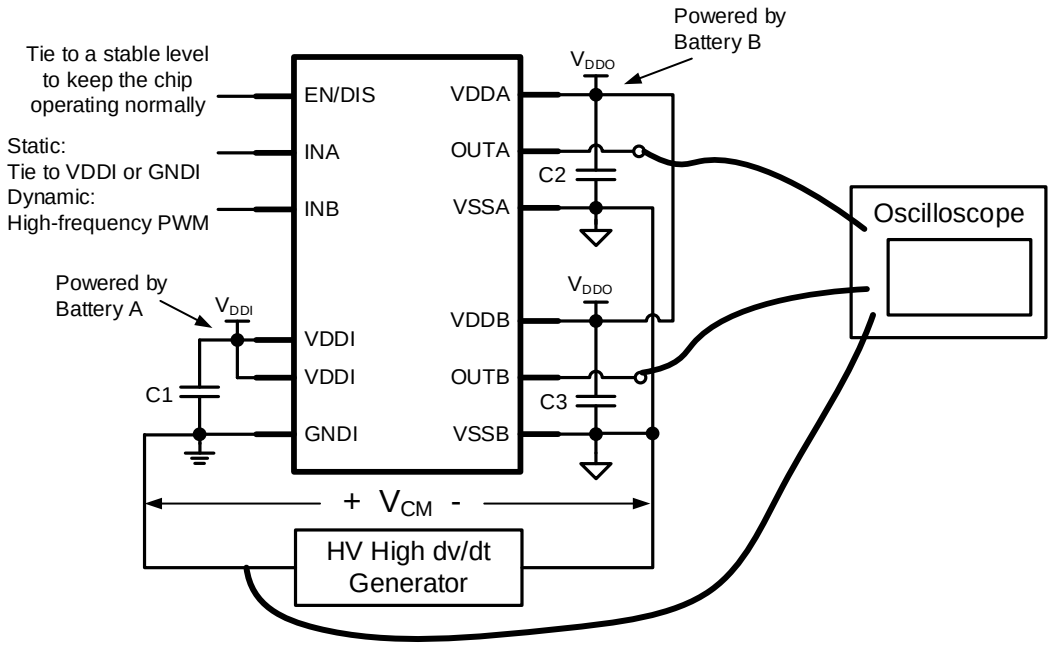

Figure 12: CMTI Test Set-Up

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APPLICATION INFORMATION

Selecting the VDDI Capacitor

The VDDI capacitor reduces the surge current drawn from the input supply, and supports current consumption for the primary logic interface and transmitter block. Since the input side's operating current is only a few mA, a 100nF ceramic capacitor with X5R or X7R dielectrics is highly recommended because of its low ESR and small temperature coefficients. For most applications, if the real supply power is far away from the VDDI pin, then it is recommended to add a >1µF bypass capacitor in parallel with this 100nF ceramic capacitor.

Selecting the VDDA/VDDB Capacitor

The VDDA/VDDB capacitor is the bypass capacitor for the output gate driver. It supports current consumption for the driving control block, maintains a stable driving voltage, and supports up to 4A of transient source current.

Given that the allowable V_{DDA}/V_{DDB} voltage ripple is $\Delta V_{DDA}/V_{DDB}$, and guarantees that the driver supply voltage cannot drop close to the UVLO level, the minimum VDDA/VDDB capacitance ($C_{VDDA/VDDB}$) can be calculated with Equation (1):

$$C_{VDDA/VDDB} = \frac{I_{VDDA/VDDB} \times \frac{1}{f_{SW}} + Q_G}{\Delta V_{DDA} / V_{DDB}} \quad (1)$$

Where $I_{VDDA/VDDB}$ is the VDDA/VDDB operating current, f_{SW} is the switching frequency, and Q_G is the power device's gate charge.

Keep in mind that the loop resistance, voltage drop, and DC bias voltage ripple impact the supply voltage. Especially for channel A, which usually operates as the high-side (HS) driver in a half-bridge converter and is powered by a bootstrap circuit, too high of a VDDA capacitance (C_{VDDA}) is not recommended as it may lead to issues, such as not charging quickly enough at system power-up or during the bootstrap cycle, or V_{DDA} remaining below its UVLO threshold and failing to power the HS driver. A 1µF capacitor is typically recommended for channel A. If channel A is powered by a special supply, a higher C_{VDDA} can be selected.

Channel B is powered by a separate supply. Because the VDDB capacitor (C_{VDDB}) must support C_{VDDA}'s charging current via the bootstrap circuit, a greater bypass capacitance can be chosen (e.g. a 10µF ceramic capacitor). It is recommended to place a secondary, high-frequency, 100nF bypass capacitor in parallel.

Selecting the Bootstrap Diode and Series Resistor

A bootstrap configuration is often applied to power the HS driver in a half-bridge converter. The bootstrap capacitor (C_{BST}) is charged through the bootstrap diode and series resistor during the low-side (LS) turn-on interval. The diode loads the high reverse voltage (greater than bus voltage) during the LS turn-on interval. To reduce the conduction losses and reverse recovery losses, a high-voltage, fast recovery diode or Schottky diode is recommended.

A bootstrap series resistor (R_{BST}) is also recommended to limit the inrush charging current, which can generate a spike on the VDDA pin. It is recommended that R_{BST} not exceed 10Ω. The estimated peak charging current can then be calculated with Equation (2):

$$I_{BST} = \frac{V_{DDA} / V_{DDB} - V_{D_BST}}{R_{BST}} \quad (2)$$

Where, V_{D_BST} is the forward voltage drop of the bootstrap diode, and R_{BST} is the bootstrap series resistor.

Selecting the Input Filter for INA/INB

The INA/INB input filter is not necessary in theory because the low-pass filter slows the PWM signal's rising/falling edge and affects the propagation delay. However, if there is significant high-frequency ringing introduced by the PCB traces, it is recommended to add a simple RC filter at the input close to the INA/INB pin.

To avoid increasing the input resistance, a resistor below 100Ω is typically recommended. When selecting the filter capacitor, ensure that the filter's cutoff frequency is at least ten times greater than f_{SW}, a capacitance of dozens of pF is typically sufficient.

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Selecting the External Driving Resistor

The external driving resistor can be applied to limit the ringing noise on the driving signal and adjust the switching speed to improve EMI performance. However, a higher driving resistance increases the switching losses, reduces system efficiency, and can introduce thermal issues. In actual applications, the turn-on and turn-off speeds can be adjusted via the respective driving resistors. Place the sink resistor in series with an anti-parallel diode, and keep it separate from the source resistor. The total driving resistance when pulling the power device low is the sum of the sink resistor in parallel with the source resistor.

The peak driving current can be used to evaluate the effect of the driving resistors. Without a driving resistor, the MP18831 can drive up to 4A of peak source and sink currents.

Considering the driving resistor, the peak source driving current for outputs A and B can be calculated with Equation (3) and Equation (4), respectively:

$$I_{OUTA_SRC} = \frac{V_{DDA}}{R_{OUTA_H} + R_{G_SRC} + R_{G(int)}} \quad (3)$$

$$I_{OUTB_SRC} = \frac{V_{DDB}}{R_{OUTB_H} + R_{G_SRC} + R_{G(int)}} \quad (4)$$

The peak sink driving current for outputs A and B can be calculated with Equation (5) and Equation (6), respectively:

$$I_{OUTA_SNK} = \frac{V_{GSA_ON}}{R_{OUTA_L} + R_{G_SRC} \,||\, R_{G_SNK} + R_{G(int)}} \quad (5)$$

$$I_{OUTB_SNK} = \frac{V_{GSB_ON}}{R_{OUTB_L} + R_{G_SRC} \,||\, R_{G_SNK} + R_{G(int)}} \quad (6)$$

Where, R_{G_SRC} is the external source resistor, R_{G_SNK} is the external sink resistor, $R_{G(INT)}$ is the power device's internal gate resistance, and V_{GSA_ON}/V_{GSB_ON} is the power device's stable gate-source voltage during the turn-on interval.

V_{GSA_ON}/V_{GSB_ON} should typically be close to V_{DDA}/V_{DDB}.

Since the driving current cannot exceed 4A, set the actual peak driving current to be the smaller value between the estimated $I_{OUTA_SRC/OUTB_SRC}$ or $I_{OUTA_SNK/OUTB_SNK}$ and 4A.

Setting the Dead Time on the DT Pin

In a half-bridge power converter, a dead time is inserted during dynamic switching transitions between the HS and LS power devices to prevent shoot-through. The MP18831's DT can be controlled via the INA/INB pins or the DT setting. The chip always selects the operating DT to be whichever delay time is longer between the driver's configured DT and the input control signal DT.

The DT setting should be determined based on the actual system requirements. Consider the real V_{GS}, V_{DS}, and switch node waveforms of both the HS and LS power devices as well as ZVS control logic. Ensure that the DT interval has sufficient margin under any possible load condition.

The MP18831's dead time setting is configured via the DT pin. Select a suitable resistor based on the dead time vs. R_{DT} curve on page 18.

Estimated Gate Driver Power Loss

The total gate driver power loss is used to estimate the thermal performance. The MP18831 must operate under the safety limiting values (see the Safety Limiting Values section on page 13 for more details).

To estimate the gate driver power loss, first calculate the chip's operation power consumption (P_{OP}) using Equation (17):

$$P_{OP} = V_{DDI} \times I_{VDDI} + V_{DDA} \times I_{VDDA} + V_{DDB} \times I_{VDDB} \quad (7)$$

The gate driver's self-power consumption is related to f_{SW} and the supply voltage. For the relationship reference between the input and output channels' current consumption vs. the operating frequency, see the Typical Characteristics section on page 15.

Next, consider the gate driver power loss during switching operation. As a conventional totem-pole (TP) gate driver, each channel of the MP18831 charges and discharges the power device's gate capacitance once during every switching cycle.

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During the charging and the discharging period, the total energy is supplied by VDDA/VDDB. If there is no external gate driver resistor, the power dissipation (P_{SW}) can be calculated with Equation (8):

$$P_{SW} = \left(V_{DDA} \times \int_0^{t_{ON}} i_{GA}(t)dt + V_{DDB} \times \int_0^{t_{ON}} i_{GB}(t)dt \right) \times f_{SW}$$
$$= \left(V_{DDA} + V_{DDB} \right) \times Q_G \times f_{SW} \quad (8)$$

Where t_{ON} is the turn-on time, and $I_{GA/GB}(t)$ is the driving current.

The behavior of the external source/sink resistors adds complexity to the dynamic power dissipation estimation.

If the driving current is not saturated to 4A within one switching cycle with external gate resistors, then P_{SW} is shared between the gate driver's internal source and sink resistances and the external gate driver resistors, based on the ratio of these series resistances. In this circumstance, P_{SW} can be calculated with Equation (9):

$$P_{SW} = \frac{V_{DDA} \times Q_G \times f_{SW}}{2} \times \left(\frac{R_{OUTA_H}}{R_{OUTA_H} + R_{G_SRC} + R_{G(int)}} + \frac{R_{OUTA_L}}{R_{OUTA_L} + R_{G_SRC} \parallel R_{G_SNK} + R_{G(int)}} \right)$$
$$+ \frac{V_{DDB} \times Q_G \times f_{SW}}{2} \times \left(\frac{R_{OUTB_H}}{R_{OUTB_H} + R_{G_SRC} + R_{G(int)}} + \frac{R_{OUTB_L}}{R_{OUTB_L} + R_{G_SRC} \parallel R_{G_SNK} + R_{G(int)}} \right) \quad (9)$$

Where t_{ON_SAT/OFF_SAT} is the turn-on/off time with a saturated 4A current output, and $V_{GSA/GSB}(t)$ is the power device's gate voltage during this saturation time.

In some conditions, the MP18831 outputs the saturated 4A current at the beginning of the turn-on/off interval. During this saturation time, the power loss (P_{SW_SAT}) can be calculated with Equation (10):

$$P_{SW_SAT} = 4A \times \int_0^{t_{ON_SAT}} \left(V_{DDA} - V_{GSA}(t) \right) dt + 4A \times \int_0^{t_{OFF_SAT}} \left(V_{GSA}(t) \right) dt$$
$$+ 4A \times \int_0^{t_{ON_SAT}} \left(V_{DDB} - V_{GSB}(t) \right) dt + 4A \times \int_0^{t_{OFF_SAT}} \left(V_{GSB}(t) \right) dt \quad (10)$$

The actual power loss is the sum of Equation (9) and Equation (10). Therefore, the total power loss dissipated in the MP18831 (P_{LOSS}) can be calculated with Equation (11):

$$P_{LOSS} = P_{OP} + P_{SW} \quad (11)$$

Multiple P_{LOSS} by the junction-to-ambient thermal resistance (θ_{JA}) to determine the junction temperature rise above the ambient temperature. Ensure that the junction temperature (T_J) is below the maximum safety temperature (T_S).

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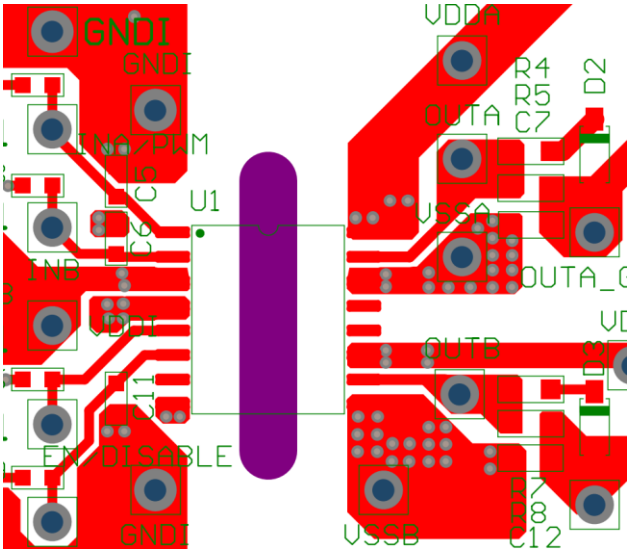
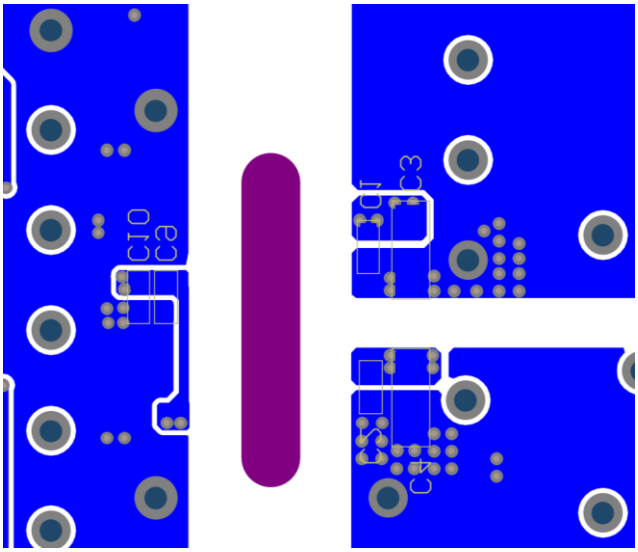
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 13 and follow the guidelines below:

1. Place the bypass/decoupling capacitors as close as possible to the VDDI/VDDA/VDDB supply pins and the corresponding grounds. For each supply pin, it is recommended to add a low-ESR/ESL, high-frequency, 100nF bypass capacitor.
2. Place the DT setting resistor and its bypass capacitor close to the DT pin.
3. If an input RC filter is used, it is recommended to place this filter close to the corresponding control pin.
4. Place the high-current paths (e.g. the supply path, drive path, and the connection between the external power device source and the VSSA/VSSB pins) very close to the driver chip with short, direct, and wide traces to minimize the parasitic inductance and avoid large transients and ringing noise.
5. It is strongly recommended to place large power and ground planes or multiple ground layers to help dissipate heat from the gate driver chip to the PCB and improve the thermal performance. Be careful when splitting the traces or coppers to allow sufficient insulation distance between the different low-/high-voltage planes.
6. Keep the driving loop from OUTA/OUTB to the power device's gate-to-source to VSSA/VSSB short and with a minimal area. Avoid placing the driving trace across different PCB layers through vias, as it can introduce parasitic inductance. Place the driver IC as close as possible to the power device.
7. Use the recommended land pattern design for each package type to ensure adequate insulation space between the primary and secondary sides. Avoid placing any components, tracks, or copper below the chip's body in any PCB layer.
8. A board cutout under the chip is not always necessary, but is recommended for the SOIC-16 package options to extend the creepage distance on the PCB surface. The LGA package's bottom side is pressed on the PCB surface, so the PCB cutout is not effective but can lead to the board being easily twisted.
9. If the driver chip is used in a half-bridge configuration, keep enough space and maximize the creepage distance between the dual channels.



Top Layer



Bottom Layer

Figure 13: Recommended PCB Layout [20]

Note:

21) This example uses a 2-layer PCB layout with the SOIC-16 WB package.

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TYPICAL APPLICATION CIRCUIT

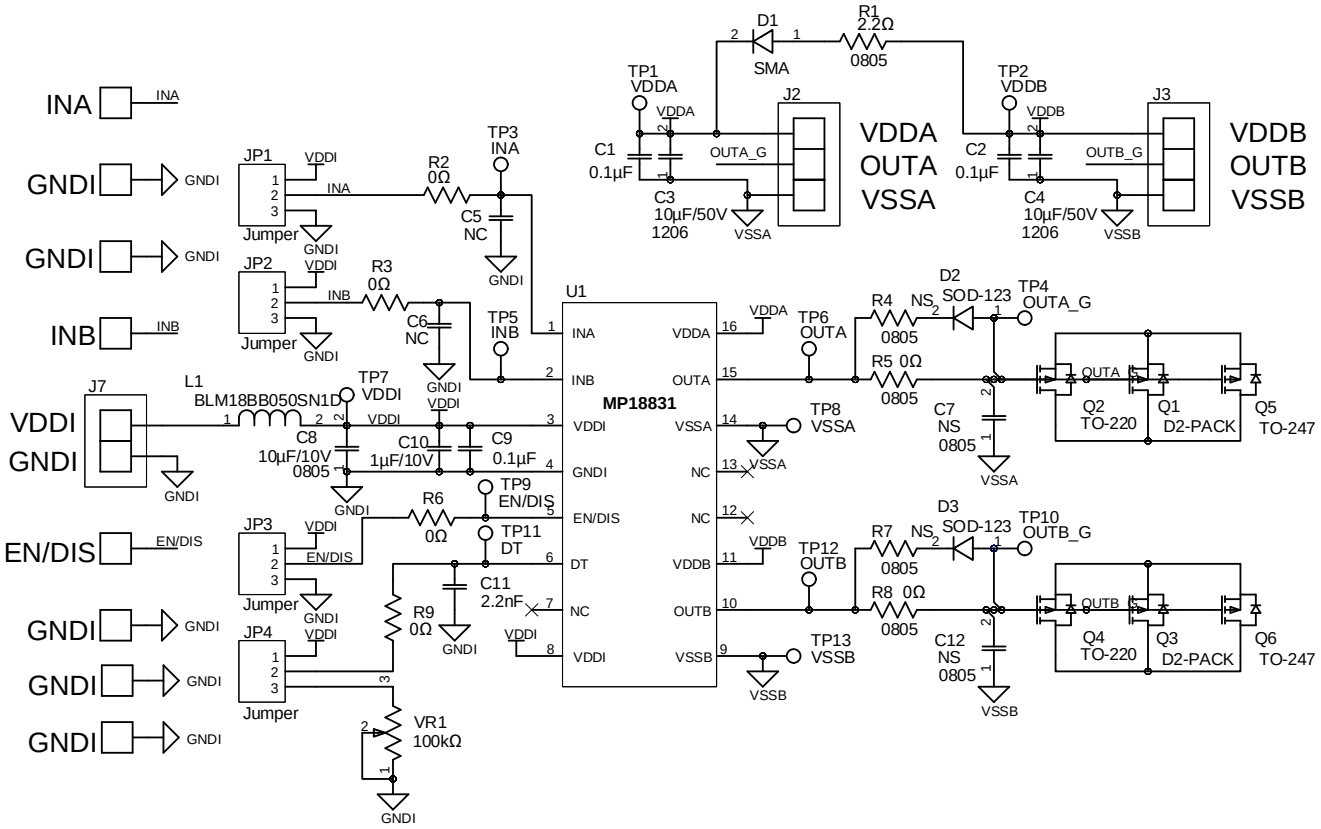

Figure 14: Typical Application Circuit

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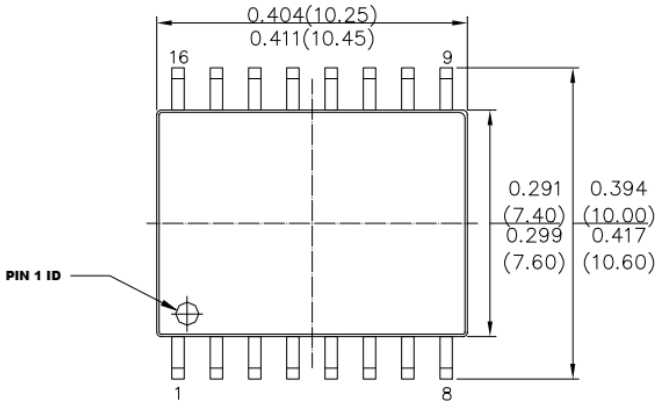
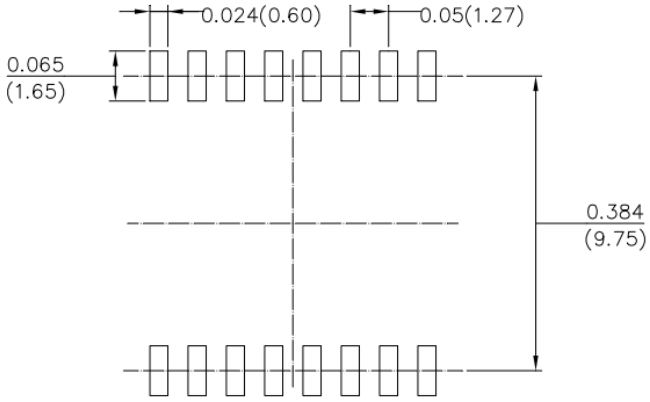
PACKAGE INFORMATION

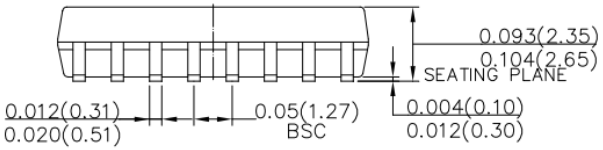
SOIC-16 WB (HV ISOLATION)



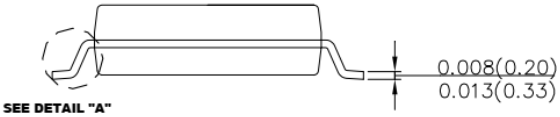
TOP VIEW



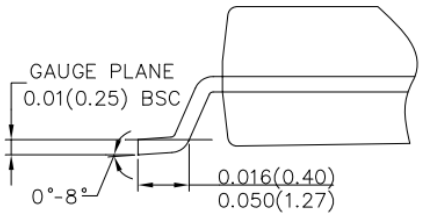
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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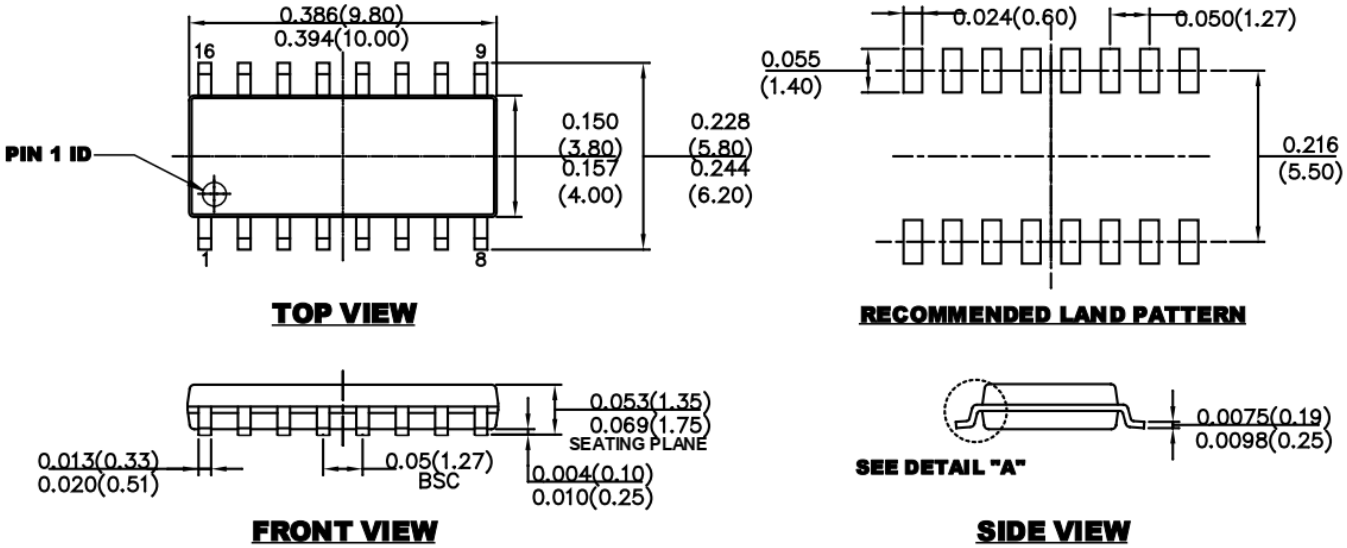
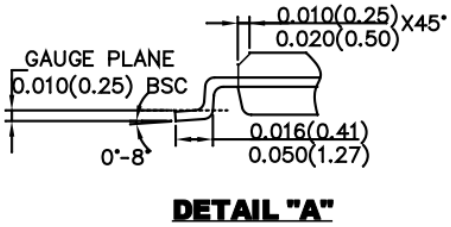
PACKAGE INFORMATION *(continued)*

SOIC-16 NB (HV ISOLATION)





NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BC.
6) DRAWING IS NOT TO SCALE.

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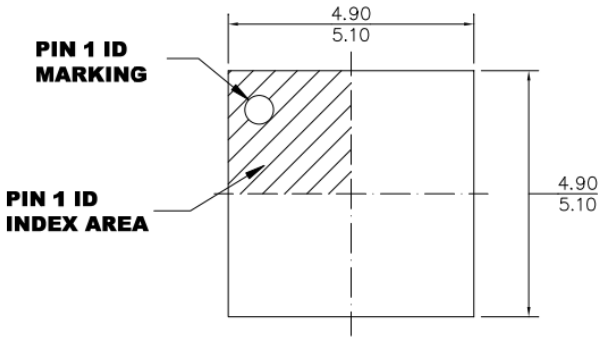
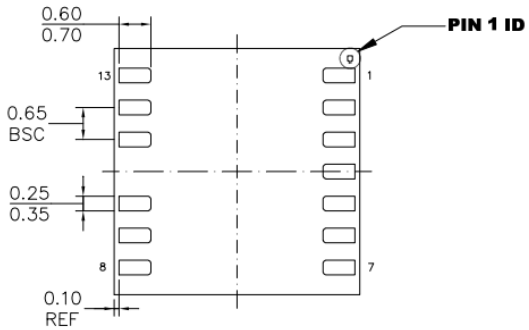
PACKAGE INFORMATION *(continued)*

LGA-13 (5mmx5mm)

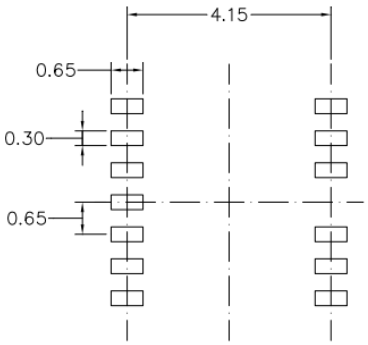


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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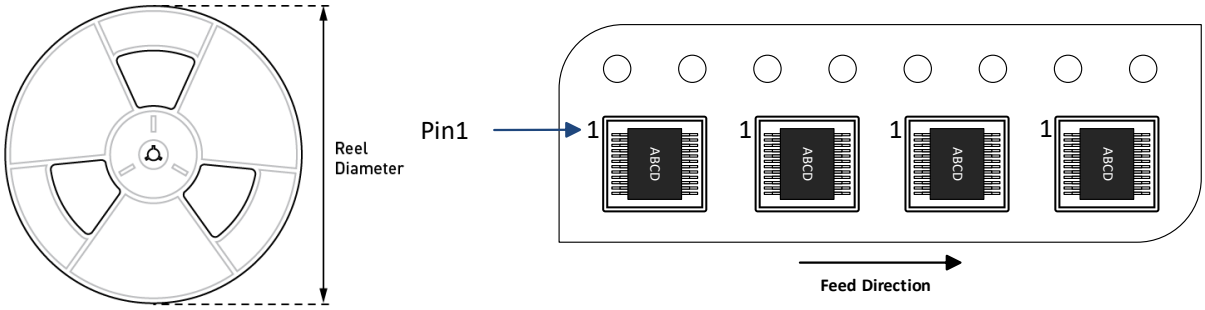
CARRIER INFORMATION

SOIC-16 NB & SOIC-16 WB



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP18831-4AGSE-Z	SOIC-16 NB	2500	50	13in	16mm	8mm
MP18831-4BGSE-Z						
MP18831-4CGSE-Z						
MP18831-4DGSE-Z						
MP18831-4EGSE-Z						
MP18831-A4AGSE-Z						
MP18831-A4BGSE-Z						
MP18831-A4CGSE-Z						
MP18831-A4DGSE-Z						
MP18831-A4EGSE-Z						
MP18831-4AGY-Z	SOIC-16 WB	1000	47	13in	24mm	12mm
MP18831-4BGY-Z						
MP18831-4CGY-Z						
MP18831-4DGY-Z						
MP18831-4EGY-Z						
MP18831-A4AGY-Z						
MP18831-A4BGY-Z						
MP18831-A4CGY-Z						
MP18831-A4DGY-Z						
MP18831-A4EGY-Z						

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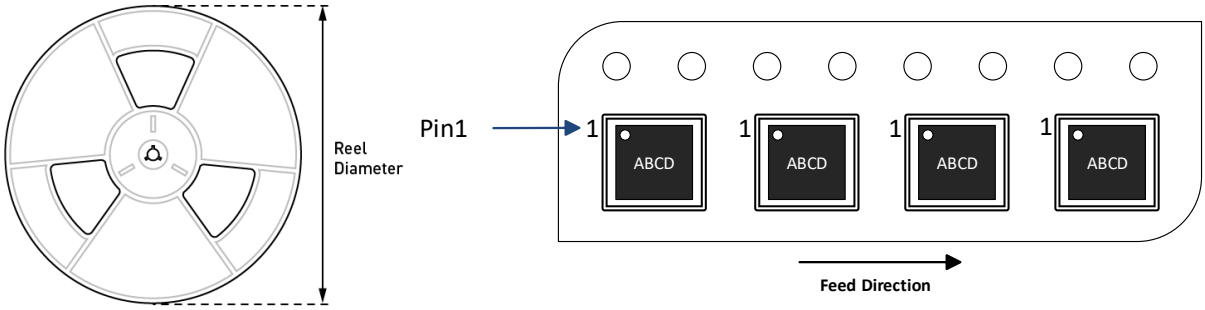
CARRIER INFORMATION *(continued)*

LGA-13 (5mmx5mm)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP18831-4AGLU-Z	LGA-13 (5mmx5mm)	5000	N/A	13in	12mm	8mm
MP18831-4BGLU-Z						
MP18831-4CGLU-Z						
MP18831-4DGLU-Z						
MP18831-4EGLU-Z						
MP18831-A4AGLU-Z						
MP18831-A4BGLU-Z						
MP18831-A4CGLU-Z						
MP18831-A4DGLU-Z						
MP18831-A4EGLU-Z						

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/26/2022	Initial Release	-

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