



DESCRIPTION

The PT9250 is an advanced single chip GPS receiver to integrate baseband, RF and flash memory into the 7mm x 10mm package making for an extremely compact design. This advanced solution offers best-in-class acquisition & tracking sensitivity, TTFF and accuracy. The PT9250 architecture uses an FFT and Matched Filter that delivers performance equivalent to more than 75,000 correlators. This represents a quantum leap forward in GPS performance. The PT9250's architecture enables unmatched TTFF at low signal levels. The PT9250 includes a powerful GPS DSP integrated with a 32-bit RISC microprocessor, 1Mb of SRAM and 4Mb flash memory. The PT9250 also integrates a built-in low power RTC circuit for low power operation and battery backup RAM for satellite information. PTC supports full reference design, demonstration system, software evaluation tools and other supporting documentation.

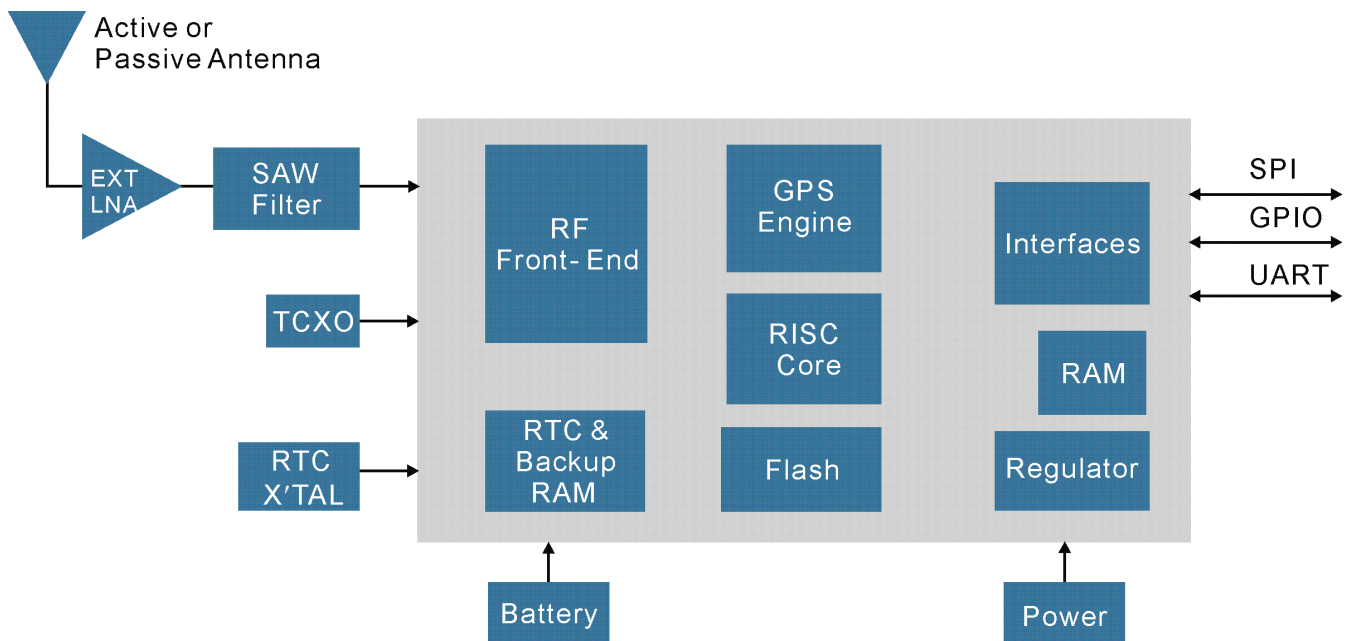
APPLICATIONS

- GPS receivers
- Vehicle navigator
- Cellular phone
- PDA
- PMP

FEATURES

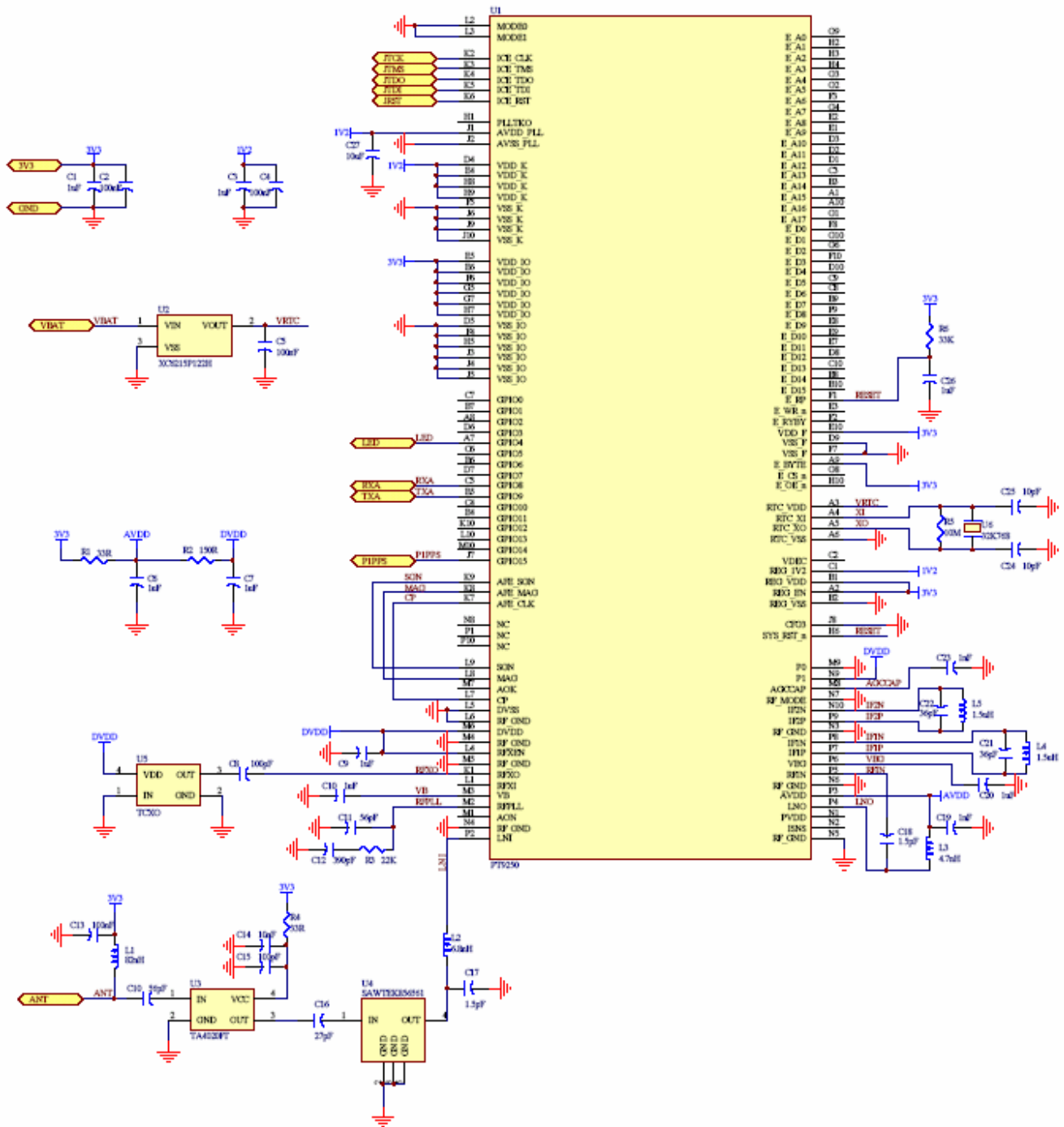
- Reception frequency: 1575.42MHz (L1 band, CA code)
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- Reference clock (TCXO) frequency: 16.368MHz or 16.369MHz
- Best-in-class acquisition and tracking sensitivity, TTFF and accuracy.
 - Tracking sensitivity -159dBm
 - Acquisition sensitivity -143dBm
- SoC to integrate major RF receiver, digital baseband and flash memory
- 48 channel acquisition and tracking engine
- 32 bits RISC CPU (MIPS)
- Internal low power real time clock
- Battery back-up SRAM
- 2-channel UART communication port
- SPI host interface
- 2 external interrupts
- Watch dog timer support
- 16 GPIOs
- 1 PPS output
- Support NMEA-0183(V3.01)
- 140 balls LFBGA
- Temperature range: -40°C/+85°C

BLOCK DIAGRAM





APPLICATION CIRCUITS





ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT9250	10mmx7mm LFBGA	PT9250

BALL CONFIGURATION

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
E_A15	REG_EN	RTC_VDD	RTC_XI	RTC_XO	RTC_VSS	GPIO4	GPIO2	E_BYTE	E_A16
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
REG_VDD	REG_VSS	E_A14	GPIO11	GPIO9	GPIO6	GPIO1	E_D14	E_D7	E_D15
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
REG_1V2	VDEC	E_A13	GPIO10	GPIO8	GPIO5	GPIO0	E_D6	E_D5	E_D13
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
E_A12	E_A11	E_A10	VDD_K	VSS_IO	GPIO3	GPIO7	E_D12	VSS_F	E_D4
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
E_A9	E_A8	E_WR_n	VDD_K	VDD_IO	VDD_IO	E_D11	E_D9	E_D10	VDD_F
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
E_RP	E_RYBY	E_A6	VSS_IO	VSS_K	VDD_IO	VSS_F	E_D0	E_D8	E_D3
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
E_A17	E_A5	E_A4	E_A7	VDD_IO	E_D2	VDD_IO	E_CS_n	E_A0	E_D1
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
PLLTKO	E_A1	E_A2	E_A3	GND_IO	SYS_RST_n	VDD_IO	VDD_K	VDD_K	E_OE_n
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
AVDD_PLIA	VSS_PLL	VSS_IO	VSS_IO	VSS_IO	VSS_K	GPIO15	CFG3	VSS_K	VSS_K
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
RFXO	ICE_CLK	ICE_TMS	ICE_TDO	ICE_TDI	ICE_RST_n	AFE_CLK	AFE_MAG	AFE_SGN	GPIO12
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10
RFXI	MODE0	MODE1	RFXEN	DVSS	RF_GND	CP	MAG	SGN	GPIO13
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
AON	RFPLL	VB	RF_GND	RF_GND	DVDD	AOK	AGCCAP	P0	GPIO14
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10
PVDD	ISNS	RFGND	RF_GND	RF_GND	RF_GND	RF_MODE	NC	P1	IF2N
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10
NC	LNI	AVDD	LNO	RFIN	VBG	IF1P	IF1N	IF2P	NC



BALL DESCRIPTION

Ball Name	I/O Type	Description
RF Interface		
SGN	O	Quantized 2nd IF “sign” bit
MAG	O	Quantized 2nd IF “magnitude” bit
AOK	O	Active antenna status output (AOK = HIGH = active antenna OK; AOK=LOW=active antenna either open or shorted)
CP	I/O	Reference clock input/output
RFXEN	I	Crystal oscillator enable pin (XEN=HIGH=enabled; XEN=LOW=disabled)
RFXI	I	Crystal oscillator input
RFXO	O	Crystal oscillator output
VB	O	Regulator (1.9V) output
RFPLL	O	Charge pump output
AON	O	Antenna switch-controlled supply voltage to active antenna
LNI	I	LNA input
ISNS	I	Antenna detector current sense input
PVDD	O	Supply voltage (active antenna)
LNO	O	LNA output
RFIN	I	Mixer input
VBG	O	Band gap reference (1.23V) output
IF1P	O	Differential first-stage IF amplifier output/differential IF AGC input
IF1N	O	
RFMODE	I	Reference frequency mode select input
AGCCAP	I/O	AGC capacitor connection. Sets the AGC time constant.
P1	I	Power-down control pins
P0	I	
RF Power Pins		
DVSS	G	Ground (digital circuitry)
DVDD	P	Supply voltage (digital circuitry)
AVDD	P	Supply voltage (analog circuitry)
RF_GND	G	Ground (analog circuitry)
Flash Interface		
E_D0 ~ E_D15	I/O	External Data bus bit 0 ~ 15
E_A0 ~ E_A17	O	External Address bus bit 0 ~ 17
E_CS_n	O	External memory chip select, active low
E_WR_n	O	External memory write signal, active low
E_OE_n	O	External memory output enable, active low
E_BYTE	I	Byte mode
E_RP	I	Reset of external memory
E_RYBY	O	Ready / Busy output
RF Chip Interface		
AFE_CLK	I	RF chip clock input
AFE_SGN	I	RF chip sign data bit
AFE_MAG	I	RF chip magnitude data bit
CPU Peripheral		
GPIO15(OPPS)	I/O	GPIO15 / One pulse per-second
GPIO14	I/O	GPIO14
GPIO13	I/O	GPIO13
GPIO12	I/O	GPIO12
GPIO11 (UATX1)	I/O	GPIO11 / UART 1 transmission data
GPIO10 (UARX1)	I/O	GPIO10 / UART 1 receive data
GPIO9 (UATX0)	I/O	GPIO9 / UART 0 transmission data
GPIO8 (UARX0)	I/O	GPIO8 / UART 0 receive data



Ball Name	I/O Type	Description
GPIO7(EXT_INT1)	I/O	GPIO7 / External interrupt input
GPIO6(EXT_INT0)	I/O	GPIO6 / External interrupt input
GPIO5	I/O	GPIO5
GPIO4	I/O	GPIO4
GPIO3 (CSIO_RDY)	I/O	GPIO3 / CSIO ready
GPIO2 (CSIO_CLK)	I/O	GPIO2 / CSIO clock
GPIO1 (CSIO_DO)	I/O	GPIO1 / CSIO data output
GPIO0 (CSIO_DI)	I/O	GPIO0 / CSIO data input
ICE Interface		
ICE_CLK	I	ICE clock
ICE_TMS	I	ICE mode select
ICE_RST_n	I	ICE reset, active low.
ICE_TDI	I	ICE data input
ICE_TDO	O	ICE data output
System Interface		
SYS_RST_n	I	System reset, active low
MODE0, MODE1	I	Test mode selection, pull low
CFG0,CFG1,CFG3	I	Configuration, pull low.
RTC_XO	O	RTC crystal clock output
RTC_XI	I	RTC crystal clock input
PLLTCKO	O	PLL test clock output
Regulator		
REG_EN	I	Regulator enable
REG_1V2	O	Regulator 1.2V output
VDEC	I	Voltage detect
Baseband Power Pins		
VDD_REG	P	3.3V power supply for regulator
VSS_REG	G	Ground for regulator
AVDD_PLL	P	Analog 1.2V power supply for PLL circuit
AVSS_PLL	G	Analog Ground for PLL
VDD_RTC	P	1.2V power supply for RTC
VSS_RTC	G	Ground for RTC
VDD_IO	P	3.3V power supply for IO
VSS_IO	G	Ground for IO
VDD_K	P	1.2V power for internal logic core
VSS_K	G	Ground for internal logic
VDD_F	P	3.3V power supply for flash
VSS_F	G	Ground for flash
NC		Open
IO Types		
I	Input(3.3V CMOS level)	
O	Output (3.3V CMOS level)	
IO	Bi-direction IO(3.3V CMOS level)	
P	Power	
G	Ground	



IMPORTANT NOTICE

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