

# ***SENSYLINK Microelectronics***

***(CA9546)***

## ***Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset***

***CA9546 is a 4-channel bidirectional translating Switch with reset input controlled by I<sup>2</sup>C/SMBus. It supports one master can access one pair or any combinations of 4 pairs of slave devices via the I<sup>2</sup>C or SMBus interface.***

***It is ideally used in Server and Telecom equipment.***

## Table of Contents

|                                                      |    |
|------------------------------------------------------|----|
| DESCRIPTION .....                                    | 3  |
| FEATURES.....                                        | 3  |
| APPLICATIONS .....                                   | 3  |
| PIN CONFIGURATIONS (TOP VIEW).....                   | 3  |
| PIN DESCRIPTION .....                                | 5  |
| FUNCTION BLOCK .....                                 | 5  |
| ORDERING INFORMATION .....                           | 6  |
| ABSOLUTE MAXIMUM RATINGS (NOTE3).....                | 7  |
| RECOMMENDED OPERATING CONDITIONS.....                | 7  |
| ELECTRICAL CHARACTERISTICS .....                     | 8  |
| I <sup>2</sup> C INTERFACE TIMING REQUIREMENTS ..... | 9  |
| 1. FUNCTION DESCRIPTIONS.....                        | 12 |
| 1.1 DEVICE ADDRESS .....                             | 12 |
| 1.2 CONTROL REGISTER .....                           | 13 |
| 1.3 RESET INPUT.....                                 | 14 |
| 1.4 POWER-ON RESET .....                             | 14 |
| 1.5 VOLTAGE TRANSLATION .....                        | 14 |
| 2. CHARACTERISTICS OF THE I <sup>2</sup> C-BUS ..... | 15 |
| 2.1 BIT TRANSFER.....                                | 15 |
| 2.2 SYSTEM CONFIGURATION.....                        | 15 |
| 2.3 ACKNOWLEDGE.....                                 | 16 |
| 2.4 BUS TRANSACTIONS.....                            | 16 |
| PACKAGE OUTLINE DIMENSIONS (SOP-16).....             | 18 |
| RECOMMEND LAND PATTERN LAYOUT (SOP-16) .....         | 19 |
| PACKAGE OUTLINE DIMENSIONS (TSSOP-16).....           | 20 |
| RECOMMEND LAND PATTERN LAYOUT (TSSOP-16).....        | 21 |
| PACKAGE OUTLINE DIMENSIONS (QFN4X4-16) .....         | 22 |
| RECOMMEND LAND PATTERN LAYOUT (QFN4X4-16).....       | 23 |
| PACKING INFORMATION.....                             | 24 |
| REVISION HISTORY.....                                | 25 |

## Figures and Tables

|                                                                 |    |                                       |    |
|-----------------------------------------------------------------|----|---------------------------------------|----|
| Figure 1. Typical application of CA9546.....                    | 4  | Figure 13. Read control register..... | 17 |
| Figure 2. CA9546 function block .....                           | 5  | Table 1 Address reference.....        | 12 |
| Figure 3. Definition of timing on the I <sup>2</sup> C-bus..... | 11 | Table 2 Command byte definition ..... | 13 |
| Figure 4. Slave address.....                                    | 12 |                                       |    |
| Figure 5. Control register.....                                 | 13 |                                       |    |
| Figure 6. Definition of RESET timing .....                      | 14 |                                       |    |
| Figure 7. Pass gate voltage versus supply voltage.....          | 14 |                                       |    |
| Figure 8. Bit transfer .....                                    | 15 |                                       |    |
| Figure 9. Definition of START and STOP condition .....          | 15 |                                       |    |
| Figure 10. System configuration.....                            | 16 |                                       |    |
| Figure 11. Acknowledgement on the I <sup>2</sup> C -bus..       | 16 |                                       |    |
| Figure 12. Write control register .....                         | 17 |                                       |    |

# Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

## Description

The chip is a 4-channel bidirectional translating switch with reset input controlled by I<sup>2</sup>C/SMBus. The upstream pair (SCL/SDA from the master) fans out to 4 downstream pairs (SCL0-3/SDA0-3 from the slaves). The CA9546 has 8-bit control register, which allows selecting any channel or any combinations of channel0-3.

The reset input pin with active low allows the chip to recover from stuck situation from any downstream pair. It can reset the I<sup>2</sup>C bus state machine, and all channels will be deselected once forcing low voltage at  $\overline{\text{RESET}}$  pin.

The chip allows using different bus voltage on each pair, like 1.8V, 2.5V or 3.3V, which can communicate with 5.0V parts by connecting external pull-up resistors to desired voltage.

Available Package: SOP-16, TSSOP-16, QFN4x4-16 package.

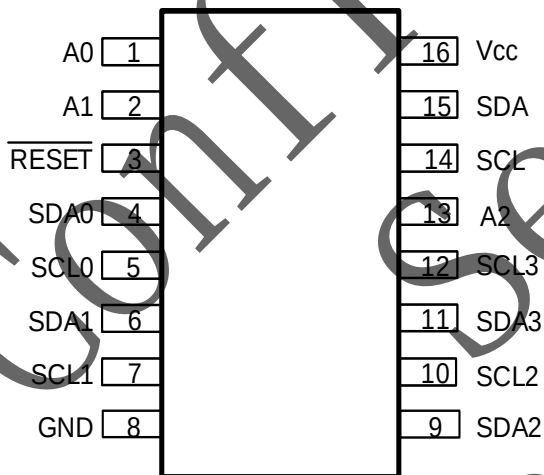
## Features

- Operation Voltage: 1.65V to 5.5V
- Standby Current: 1.5uA (Max.)
- 1-of-4 bidirectional translating switches between 1.8V, 2.5V, 3.3V and 5.0V
- Compatible with SMBus and I<sup>2</sup>C interface
- I<sup>2</sup>C Speed up to 1.0MHz (Fast mode+)
- Up to 8 slave addresses
- $\overline{\text{RESET}}$  input with active low
- 5.5V tolerant inputs
- Channel0-3 or any combination selection by Control Register
- Support hot insertion
- No Glitch during Power-up
- Noise Filter on SCL/SDA inputs
- Temperature Range: -40°C to 85°C

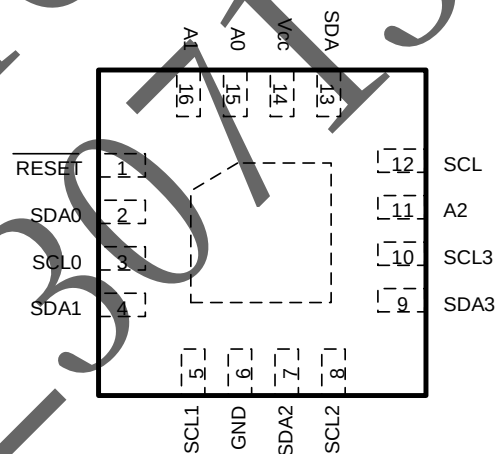
## Applications

- Server, Notebook PC
- Telecom equipment

## PIN Configurations (Top View)



SOP-16/TSSOP-16(Package code M/MT)



QFN4x4-16(Package code QN)

## Typical Application

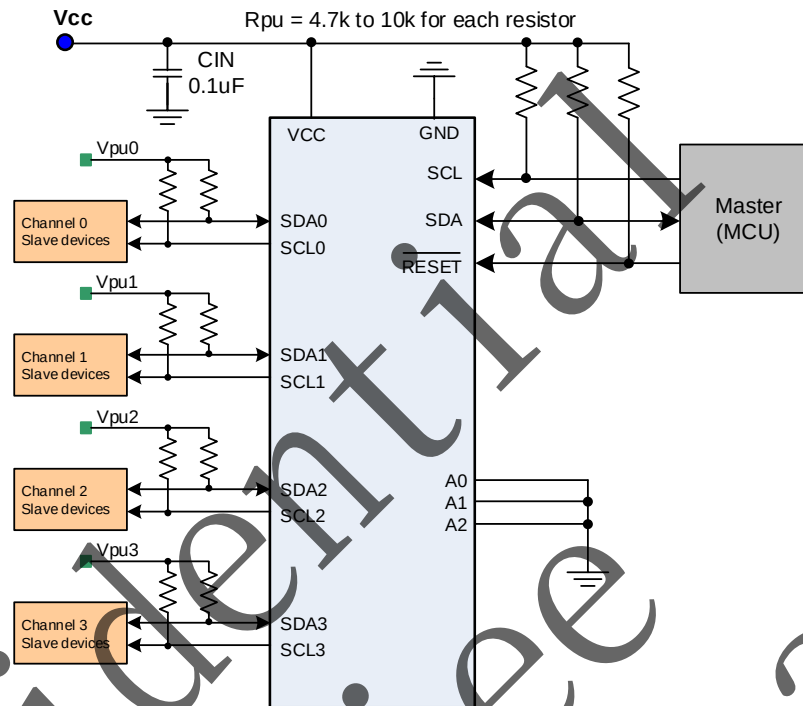


Figure 1. Typical application of CA9546

# Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

## Pin Description

| PIN Name | PIN No.            |           | Description                                                                       |
|----------|--------------------|-----------|-----------------------------------------------------------------------------------|
|          | SOP-16<br>TSSOP-16 | QFN4x4-16 |                                                                                   |
| A0       | 1                  | 15        | Slave addresses setup pin input 0 , Connect directly to Vcc or ground             |
| A1       | 2                  | 16        | Slave addresses setup pin input 1 , Connect directly to Vcc or ground             |
| RESET    | 3                  | 1         | Reset input with active low.                                                      |
| SDA0     | 4                  | 2         | Serial data of channel 0, connect to Vpu0 <sup>(1)</sup> via a pull-up resistor.  |
| SCL0     | 5                  | 3         | Serial clock of channel 0, connect to Vpu0 <sup>(1)</sup> via a pull-up resistor. |
| SDA1     | 6                  | 4         | Serial data of channel 1, connect to Vpu1 <sup>(1)</sup> via a pull-up resistor.  |
| SCL1     | 7                  | 5         | Serial clock of channel 1, connect to Vpu1 <sup>(1)</sup> via a pull-up resistor. |
| GND      | 8                  | 6         | Ground pin.                                                                       |
| SDA2     | 9                  | 7         | Serial data of channel 2, connect to Vpu2 <sup>(1)</sup> via a pull-up resistor.  |
| SCL2     | 10                 | 8         | Serial clock of channel 2, connect to Vpu2 <sup>(1)</sup> via a pull-up resistor. |
| SDA3     | 11                 | 9         | Serial data of channel 3, connect to Vpu3 <sup>(1)</sup> via a pull-up resistor.  |
| SCL3     | 12                 | 10        | Serial clock of channel 3, connect to Vpu3 <sup>(1)</sup> via a pull-up resistor. |
| A2       | 13                 | 11        | Slave addresses setup pin input 2 , Connect directly to Vcc or ground             |
| SCL      | 14                 | 12        | Digital interface clock input pin, need a pull-up resistor to Vcc.                |
| SDA      | 15                 | 13        | Digital interface data input or output pin, need a pull-up resistor to Vcc.       |
| Vcc      | 16                 | 14        | Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground           |

[1] Vpu0-Vpu3 are the pull-up reference voltage for the associated data line.

## Function Block

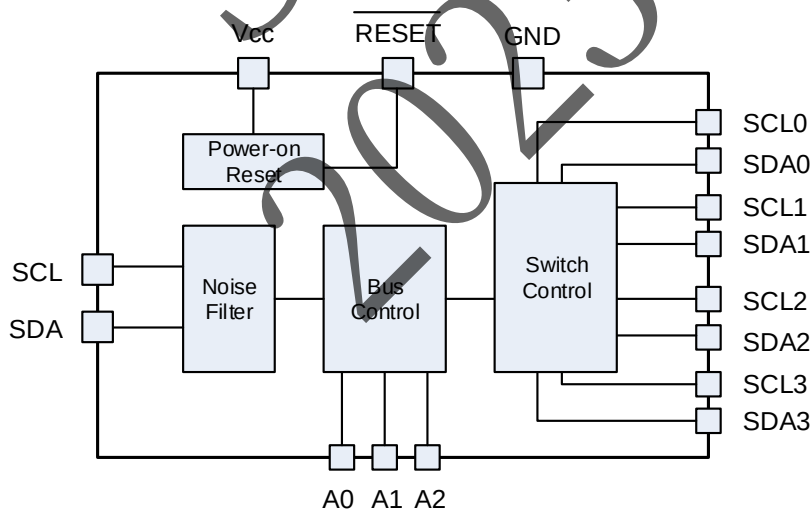


Figure 2. CA9546 function block

# Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

## Ordering Information

**CA9546**
**X**
**X**

### Package Type

M : SOP-16

MT : TSSOP-16

QN : QFN4x4-16

### Packing

R : Tape &amp; Reel

| Order PN  | Green <sup>1</sup> | Package   | Marking ID <sup>2</sup> | Packing     | MPQ   | Operation Temperature |
|-----------|--------------------|-----------|-------------------------|-------------|-------|-----------------------|
| CA9546MR  | Halogen free       | SOP-16    | 9546<br>YWWAXX          | Tape & Reel | 4,000 | -40°C ~ +85°C         |
| CA9546MTR | Halogen free       | TSSOP-16  | 9546<br>YWWAXX          | Tape & Reel | 4,000 | -40°C ~ +85°C         |
| CA9546QNR | Halogen free       | QFN4x4-16 | 9546<br>YWWAXX          | Tape & Reel | 5,000 | -40°C ~ +85°C         |

### Notes

1. Based on ROHS V2012 spec, Halogen free covers lead free. So most package types Sensylink offers only states halogen free, instead of lead free.

2. Marking ID includes 2 rows of characters. In general, the 1<sup>st</sup> row of characters are part number, and the 2<sup>nd</sup> row of characters are date code plus production information.

## Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

### Absolute Maximum Ratings (Note3)

| Parameter                                | Symbol                                                                                       | Value      | Unit |
|------------------------------------------|----------------------------------------------------------------------------------------------|------------|------|
| Supply Voltage                           | V <sub>CC</sub> to GND                                                                       | -0.5 to 7  | V    |
| SDA, SCL, A0-A2 Voltage                  | V <sub>SDA</sub> /V <sub>SCL</sub> /V <sub>A0</sub> /V <sub>A1</sub> /V <sub>A2</sub> to GND | -0.5 to 7  | V    |
| RESET Voltage                            | V <sub>RESET</sub> to GND                                                                    | -0.5 to 7  | V    |
| SDA0-3, SCL0-3 Voltage                   | V <sub>SDA0-3</sub> /V <sub>SCL0-3</sub> to GND                                              | -0.5 to 7  | V    |
| Storage temperature Range                | T <sub>STG</sub>                                                                             | -65 to 150 | °C   |
| Lead Temperature (Soldering, 10 Seconds) | T <sub>LEAD</sub>                                                                            | 260        | °C   |
| Maximum Junction Temperature             | T <sub>J(Max)</sub>                                                                          | 125        | °C   |
| ESD MM                                   | ESD <sub>MM</sub>                                                                            | ±200       | V    |
| ESD HBM                                  | ESD <sub>HBM</sub>                                                                           | ±4000      | V    |
| ESD CDM                                  | ESD <sub>CDM</sub>                                                                           | ±1000      | V    |

#### Note3

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

### Recommended Operating Conditions

| Parameter                           | Symbol          | Value      | Unit |
|-------------------------------------|-----------------|------------|------|
| Supply Voltage                      | V <sub>CC</sub> | 1.65 ~ 5.5 | V    |
| Ambient Operation Temperature Range | T <sub>A</sub>  | -40 ~ +85  | °C   |

# Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

## Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

| Parameter                    | Symbol             | TEST CONDITIONS                                                                                             | MIN                  | Typ <sup>(1)</sup> | MAX                  | UNIT |
|------------------------------|--------------------|-------------------------------------------------------------------------------------------------------------|----------------------|--------------------|----------------------|------|
| Supply Voltage               | V <sub>CC</sub>    |                                                                                                             | 1.65                 |                    | 5.5                  | V    |
| Supply Current               | I <sub>CC</sub>    | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> <sup>(2)</sup> = V <sub>CC</sub> or GND; f <sub>SCL</sub> = 100 kHz |                      | 5                  | 20                   | uA   |
|                              |                    | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND; f <sub>SCL</sub> = 100 kHz                |                      | 9                  | 30                   | uA   |
| Standby current              | I <sub>stb</sub>   | V <sub>CC</sub> = 3.6 V; no load; V <sub>I</sub> = V <sub>CC</sub> or GND                                   |                      | 0.5                | 1                    | uA   |
|                              |                    | V <sub>CC</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>CC</sub> or GND                                   |                      | 0.8                | 1.5                  | uA   |
| Power-on reset voltage       | V <sub>POR</sub>   | no load; V <sub>I</sub> = V <sub>CC</sub> or GND                                                            |                      | 1.4                | 1.55                 | V    |
| LOW-level input voltage      | V <sub>IL</sub>    | SCL, SDA                                                                                                    | -0.5                 |                    | 0.3* V <sub>CC</sub> | V    |
|                              |                    | A2-A0, RESET                                                                                                | -0.5                 |                    | 0.3* V <sub>CC</sub> | V    |
| HIGH-level input voltage     | V <sub>IH</sub>    | SCL, SDA                                                                                                    | 0.7* V <sub>CC</sub> |                    | 6                    | V    |
|                              |                    | A2-A0, RESET                                                                                                | 0.7* V <sub>CC</sub> |                    | V <sub>CC</sub> +0.5 | V    |
| LOW-level input current      | I <sub>IL</sub>    | V <sub>I</sub> = GND                                                                                        | -1                   |                    | 1                    | uA   |
| HIGH-level input current     | I <sub>IH</sub>    | V <sub>I</sub> = V <sub>CC</sub>                                                                            | -1                   |                    | 1                    | uA   |
| SDA LOW-level output current | I <sub>OL</sub>    | V <sub>OL</sub> = 0.4 V                                                                                     | 3                    |                    |                      | mA   |
|                              |                    | V <sub>OL</sub> = 0.6 V                                                                                     | 6                    |                    |                      | mA   |
| Input capacitance            | C <sub>i</sub>     | A2-A0; V <sub>I</sub> = V <sub>CC</sub> or GND                                                              |                      | 4                  |                      | pF   |
|                              |                    | RESET; V <sub>I</sub> = V <sub>CC</sub> or GND                                                              |                      | 4                  |                      | pF   |
|                              |                    | SCL V <sub>I</sub> = V <sub>CC</sub> or GND, Switch OFF                                                     |                      | 20                 |                      | pF   |
| Switch-on resistance         | R <sub>ON</sub>    | V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 15 mA, V <sub>CC</sub> = 3.3V                                      | 5                    | 12                 | 30                   | Ω    |
|                              |                    | V <sub>O</sub> = 0.4 V, I <sub>O</sub> = 15 mA, V <sub>CC</sub> = 5.5V                                      | 4                    | 8                  | 20                   | Ω    |
| Switch output voltage        | V <sub>O(sw)</sub> | V <sub>I</sub> (sw) = V <sub>CC</sub> = 1.8 V; I <sub>O</sub> (sw) = -100uA                                 |                      | 0.95               |                      | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 1.65 V to 1.95 V; I <sub>O</sub> (sw) = -100uA                      | 0.45                 |                    | 1.5                  | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 2.5 V; I <sub>O</sub> (sw) = -100uA                                 |                      | 1.4                |                      | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>O</sub> (sw) = -100uA                        | 0.9                  |                    | 2                    | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 3.3V; I <sub>O</sub> (sw) = -100uA                                  |                      | 1.95               |                      | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 3.0V to 3.6 V; I <sub>O</sub> (sw) = -100uA                         | 1.35                 |                    | 2.8                  | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 5.0V; I <sub>O</sub> (sw) = -100uA                                  |                      | 3.3                |                      | V    |
|                              |                    | V <sub>I</sub> (sw) = V <sub>CC</sub> = 4.5V to 5.5 V; I <sub>O</sub> (sw) = -100uA                         | 2.4                  |                    | 4.5                  | V    |

[1] All typical values are at nominal supply voltage (V<sub>CC</sub>=3.3V), T<sub>A</sub> = 25°C.

[2] RESET =V<sub>CC</sub> when all other input V<sub>I</sub>=GND.

## Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

### I<sup>2</sup>C Interface Timing Requirements

Over recommended operating free-air temperature range (unless otherwise noted)

| Parameter                                                                      | Symbol              | TEST CONDITIONS               | MIN  | Typ | MAX  | UNIT |
|--------------------------------------------------------------------------------|---------------------|-------------------------------|------|-----|------|------|
| I <sup>2</sup> C clock frequency                                               | f <sub>SCL</sub>    | Standard-mode                 | 0    |     | 100  | kHz  |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 0    |     | 400  | kHz  |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0    |     | 1000 | kHz  |
| I <sup>2</sup> C bus free time between stop and start                          | t <sub>BUF</sub>    | Standard-mode                 | 4.7  |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 1.3  |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0.5  |     |      | us   |
| I <sup>2</sup> C start or repeated start condition hold                        | t <sub>HD;STA</sub> | Standard-mode                 | 4.0  |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 0.6  |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0.26 |     |      | us   |
| I <sup>2</sup> C start or repeated start condition setup                       | t <sub>SU;STA</sub> | Standard-mode                 | 4.7  |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 0.6  |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0.26 |     |      | us   |
| I <sup>2</sup> C stop condition setup                                          | t <sub>SU;STO</sub> | Standard-mode                 | 4.0  |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 0.6  |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0.26 |     |      | us   |
| Valid data time of ACK condition<br>(ACK signal from SCL low to SDA (out) low) | t <sub>VD;ACK</sub> | Standard-mode                 |      |     | 3.45 | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      |      |     | 0.9  | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> |      |     | 0.45 | us   |
| I <sup>2</sup> C serial-data hold time                                         | t <sub>HD;DAT</sub> | Standard-mode                 | 0    |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 0    |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0    |     |      | us   |
| I <sup>2</sup> C Valid data time<br>(SCL low to SDA output valid)              | t <sub>VD;DAT</sub> | Standard-mode                 |      |     | 3.45 | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      |      |     | 0.9  | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> |      |     | 0.45 | us   |
| I <sup>2</sup> C serial-data setup time                                        | t <sub>SU;DAT</sub> | Standard-mode                 | 250  |     |      | ns   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 100  |     |      | ns   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 50   |     |      | ns   |
| I <sup>2</sup> C clock low time                                                | t <sub>LOW</sub>    | Standard-mode                 | 4.7  |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 1.3  |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0.5  |     |      | us   |
| I <sup>2</sup> C clock high time                                               | t <sub>HIGH</sub>   | Standard-mode                 | 4.0  |     |      | us   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      | 0.6  |     |      | us   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> | 0.26 |     |      | us   |
| I <sup>2</sup> C input fall time                                               | t <sub>F</sub>      | Standard-mode                 |      |     | 300  | ns   |
|                                                                                |                     | Fast-mode <sup>(1)</sup>      |      |     | 300  | ns   |
|                                                                                |                     | Fast-mode Plus <sup>(2)</sup> |      |     | 120  | ns   |

# Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

## I<sup>2</sup>C Interface Timing Requirements (continued)

| Parameter                                                                                     | Symbol                 | TEST CONDITIONS                                | MIN | Typ | MAX  | UNIT |
|-----------------------------------------------------------------------------------------------|------------------------|------------------------------------------------|-----|-----|------|------|
| I <sup>2</sup> C output fall time<br>(SDA out, 4.7kΩ R <sub>pull</sub> , 10-pF to 400-pF bus) | t <sub>OF</sub>        | Standard-mode                                  |     |     | 300  | ns   |
|                                                                                               |                        | Fast-mode <sup>(1)</sup>                       |     |     | 300  | ns   |
|                                                                                               |                        | Fast-mode Plus <sup>(2)</sup>                  |     |     | 120  | ns   |
| I <sup>2</sup> C input rise time                                                              | t <sub>R</sub>         | Standard-mode                                  |     |     | 1000 | ns   |
|                                                                                               |                        | Fast-mode <sup>(1)</sup>                       |     |     | 300  | ns   |
|                                                                                               |                        | Fast-mode Plus <sup>(2)</sup>                  |     |     | 120  | ns   |
| I <sup>2</sup> C spike time                                                                   | t <sub>sp</sub>        | SDA, SCL pin                                   |     |     | 50   | ns   |
| data valid time                                                                               | t <sub>vdL(Data)</sub> | [high to low] SCL low to SDA output low valid  |     |     | 1    | ns   |
|                                                                                               | t <sub>vdH(Data)</sub> | [low to high] SCL low to SDA output high valid |     |     | 0.6  | ns   |
| data valid acknowledge time                                                                   | t <sub>VD;ACK</sub>    | ACK signal from SCL low to SDA (out) low       |     |     | 1    | us   |
| <b>Reset Digital Interface</b>                                                                |                        |                                                |     |     |      |      |
| LOW-level reset time                                                                          | t <sub>WL</sub>        |                                                | 6   |     |      | ns   |
| reset time                                                                                    | t <sub>rst</sub>       |                                                |     |     | 500  | ns   |
| recovery time to START condition                                                              | t <sub>REC(STA)</sub>  |                                                |     | 0   |      | ns   |

Note:

(1) In Fast-mode, the external pull-up resistance of SDA and SCL is typically 4.7 KΩ.

(2) In Fast-mode Plus, the external pull-up resistance of SDA and SCL is typically 0.51 KΩ.

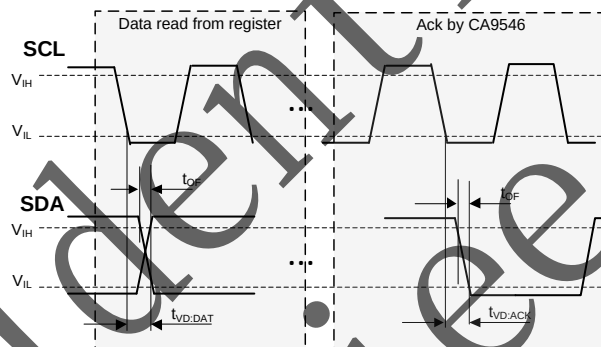
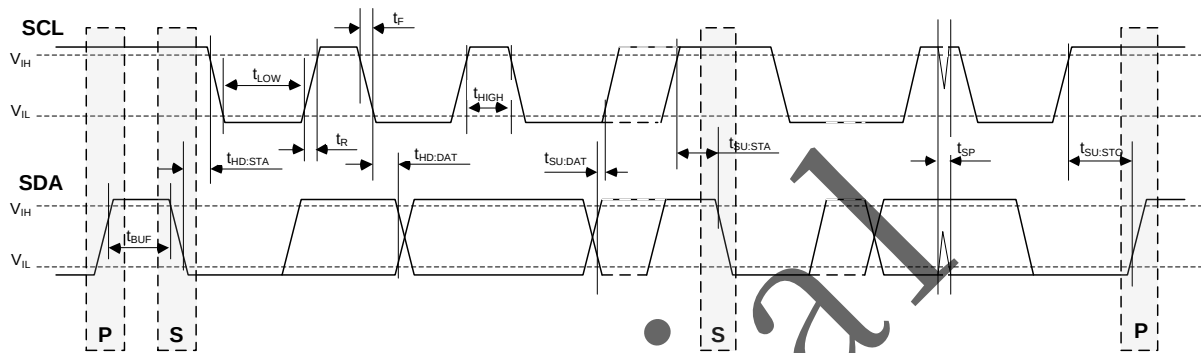


Figure 3. Definition of timing on the I<sup>2</sup>C-bus

## 1. Function Descriptions

The CA9546 is a 4-channel, bidirectional translating I<sup>2</sup>C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SCL0/SDA0-SCL3/SDA3. Any individual downstream channel can be selected as well as any combination of the four channels.

The device offers an active-low  $\overline{\text{RESET}}$  input which resets the state machine and allows the CA9546 to recover when one of the downstream I<sup>2</sup>C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply Vcc, also known as a power-on reset (POR). Both the  $\overline{\text{RESET}}$  function and a POR will cause all channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C master device that is switched to communicate with multiple I<sup>2</sup>C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0, A1 and A2 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The CA9546 may also be used for voltage translation, allowing the use of different bus voltages on each SCLx/SDAx pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

### 1.1 Device address

Following a START condition, the bus master must output the address of the slave which it is accessing. The address of the CA9546 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

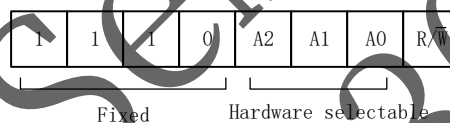


Figure 4. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation. Table 1 shows the CA9546 address reference.

Table 1 Address reference

| INPUTS |    |    | I <sup>2</sup> C BUS SLAVE ADDRESS |      |
|--------|----|----|------------------------------------|------|
| A2     | A1 | A0 | Write                              | Read |
| L      | L  | L  | 0xe0                               | 0xe1 |
| L      | L  | H  | 0xe2                               | 0xe3 |
| L      | H  | L  | 0xe4                               | 0xe5 |
| L      | H  | H  | 0xe6                               | 0xe7 |
| H      | L  | L  | 0xe8                               | 0xe9 |
| H      | L  | H  | 0xea                               | 0xeb |
| H      | H  | L  | 0xec                               | 0xed |
| H      | H  | H  | 0xee                               | 0xef |

## Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

### 1.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the CA9546 (see Figure 5), which will be stored in the control register. If multiple bytes are received by the CA9546, it will save the last byte received. This register can be written and read via the I<sup>2</sup>C -bus. Table 2 shows the CA9546 command byte definition.

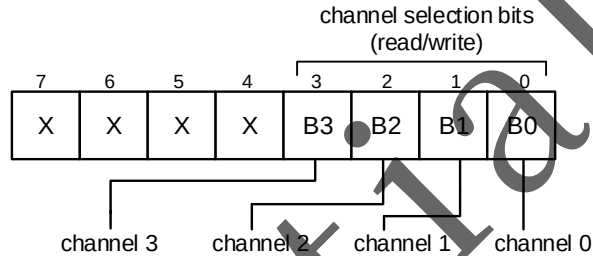


Figure 5. Control register

One or several SCLx/SDAx downstream pair, or channel, is selected by the contents of the control register. This register is written after the CA9546 has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I<sup>2</sup>C -bus. This ensures that all SCLx/SDAx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection. the 4 MSBs are invalid bits and reads 0 in any case. Table 2 shows the CA9546 command byte definition.

Table 2 Command byte definition

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Command                                              |
|----|----|----|----|----|----|----|----|------------------------------------------------------|
| x  | x  | x  | x  | x  | x  | x  | 0  | channel 0 disabled                                   |
| x  | x  | x  | x  | x  | x  | x  | 1  | channel 0 enabled                                    |
| x  | x  | x  | x  | x  | x  | 0  | x  | channel 1 disabled                                   |
| x  | x  | x  | x  | x  | x  | 1  | x  | channel 1 enabled                                    |
| x  | x  | x  | x  | x  | 0  | x  | x  | channel 2 disabled                                   |
| x  | x  | x  | x  | x  | 1  | x  | x  | channel 2 enabled                                    |
| x  | x  | x  | x  | 0  | x  | x  | x  | channel 3 disabled                                   |
| x  | x  | x  | x  | 1  | x  | x  | x  | channel 3 enabled                                    |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | no channel selected;<br>power-up/reset default state |

**Remark:** Several channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channel 0 and channel 3 are disabled and channel 1 and channel 2 are enabled. Care should be taken not to exceed the maximum bus capacitance.

## Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

### 1.3 $\overline{\text{RESET}}$ input

The  $\overline{\text{RESET}}$  input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of  $t_{w(\text{rst})L}$ , the CA9546 resets its registers and I<sup>2</sup>C -bus state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to Vcc through a pull-up resistor(see Figure 1).

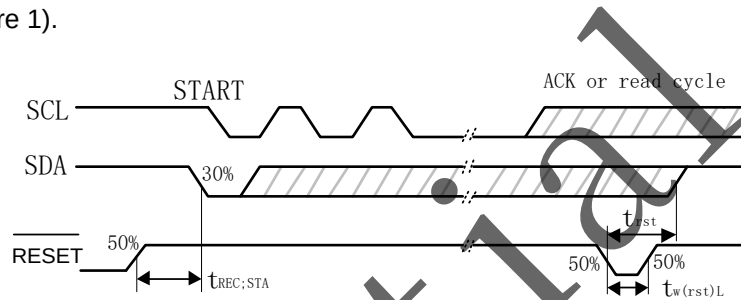


Figure 6. Definition of  $\overline{\text{RESET}}$  timing

### 1.4 Power-on reset

When power is applied to Vcc, an internal Power-On Reset (POR) holds the CA9546 in a reset condition until Vcc has reached V<sub>POR</sub>. At this point, the reset condition is released and the CA9546 register and I<sup>2</sup>C -bus state machine is initialized to their default states (all zeroes) causing all the channels to be deselected.

### 1.5 Voltage translation

The pass gate transistors of the CA9546 are constructed such that the Vcc voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C -bus to another.

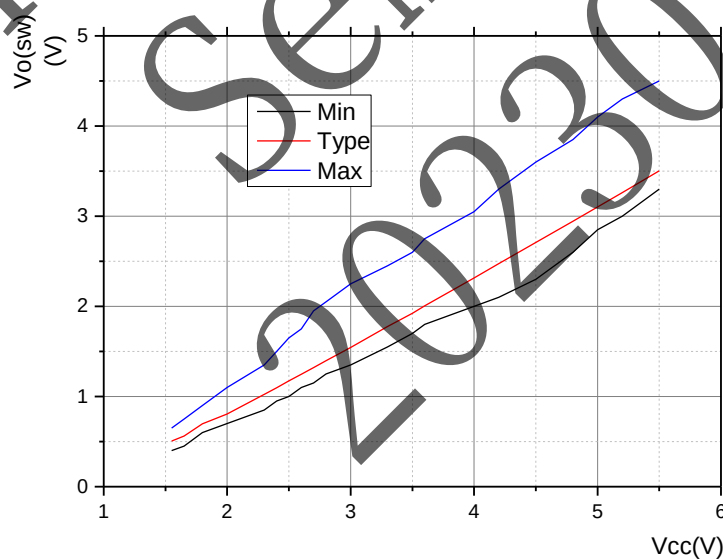


Figure 7. Pass gate voltage versus supply voltage

Figure 7 shows the voltage characteristics of the pass gate transistors (note that the CA9546 is only tested at the points specified in “Electrical Characteristics” of this data sheet). In order for the CA9546 to act as a voltage translator, the Vo(sw) voltage should be equal to, or lower than the lowest bus voltage.

For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then

$V_{o(sw)}$  should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 7 we see that  $V_{o(sw)}(max)$  will be at 2.7 V when the CA9546 supply voltage is 3.5 V or lower, so the CA9546 supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels.

## 2. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C -bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 2.1. Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 8).

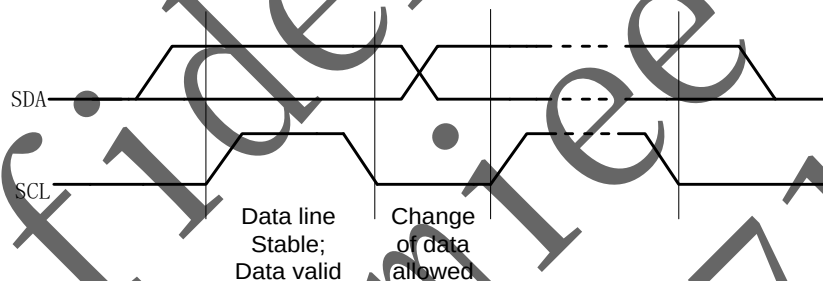


Figure 8. Bit transfer

### 2.2. START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

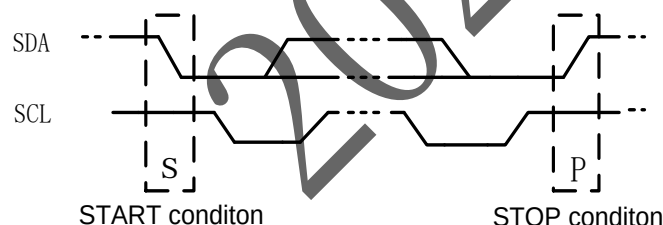


Figure 9. Definition of START and STOP condition

### 2.3. System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Figure 10).

## Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

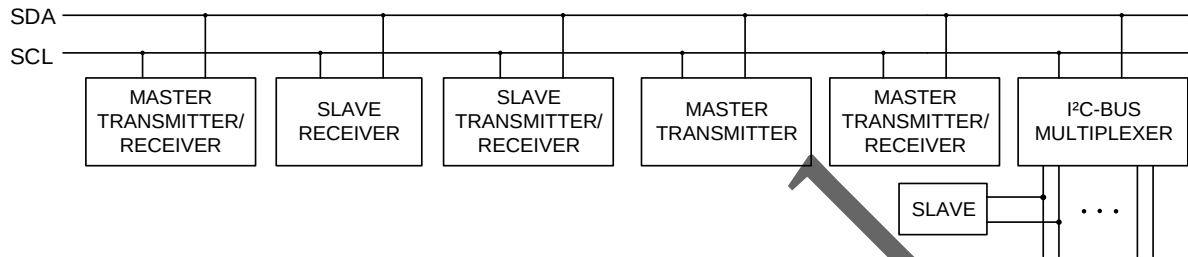


Figure 10. System configuration

### 2.4. Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

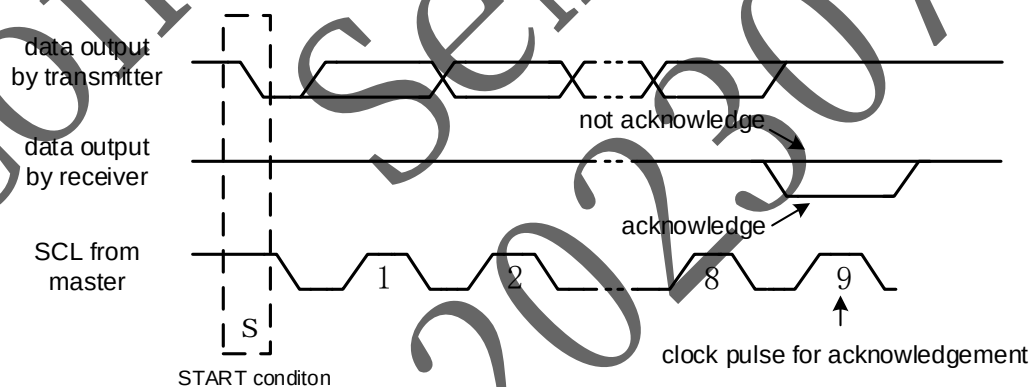


Figure 11. Acknowledgement on the I<sup>2</sup>C -bus

### 2.5. Bus transactions

Data is transmitted to the CA9546 control register using the Write mode as shown in Figure 12. Data is read from CA9546 using the Read mode as shown in Figure 13. Stop condition is necessary.

# Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

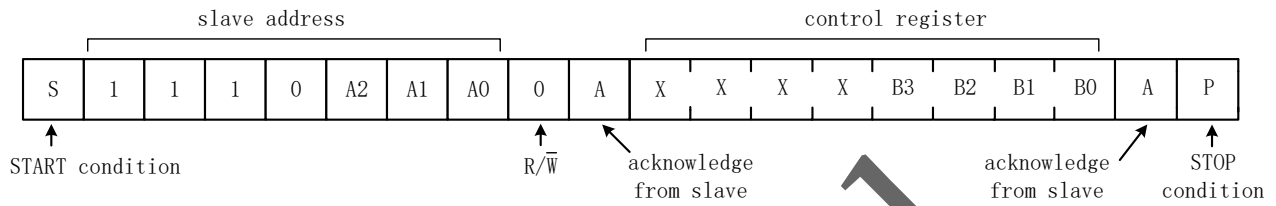


Figure 12. Write control register

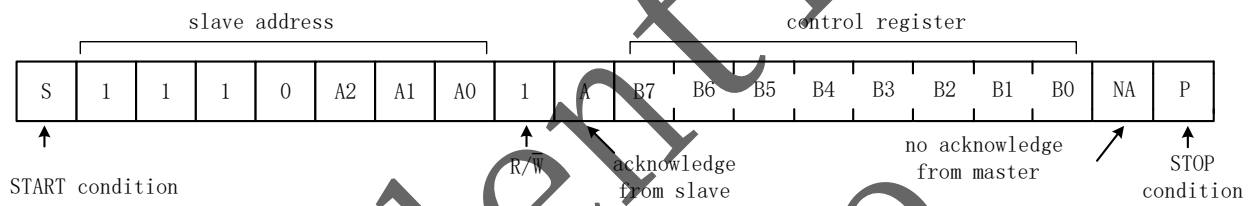
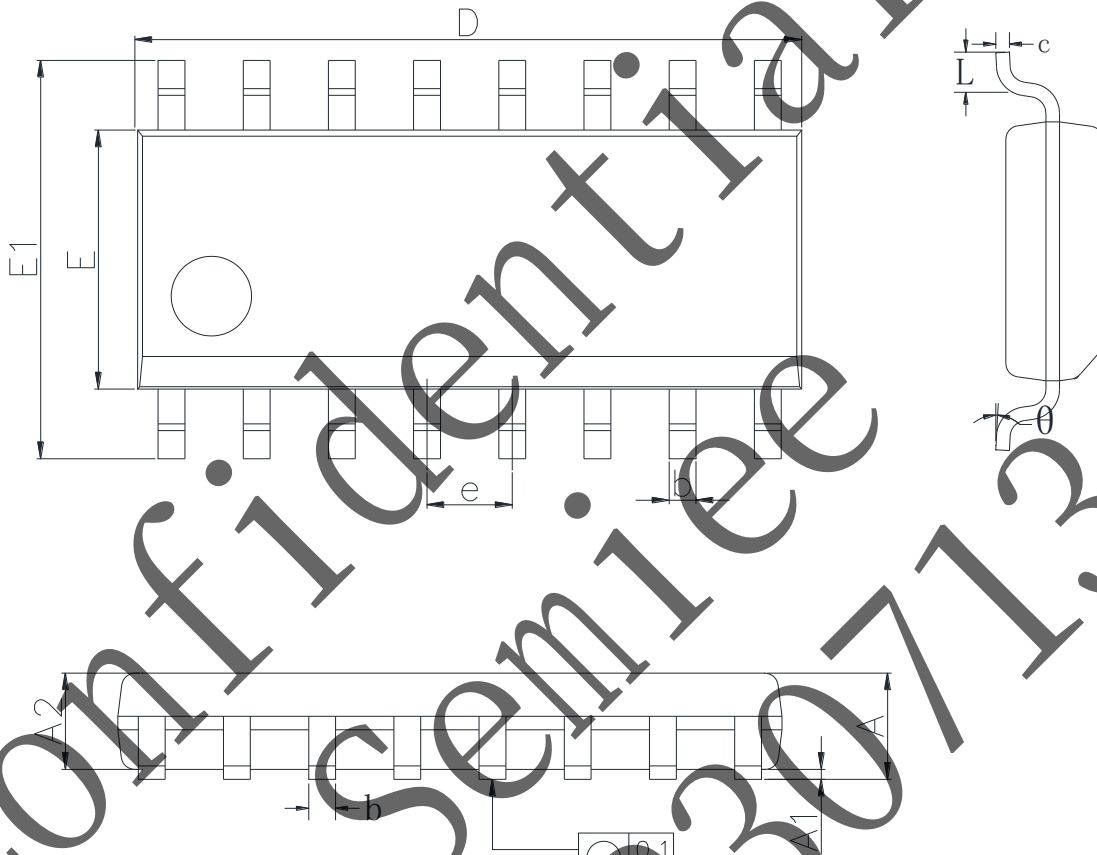
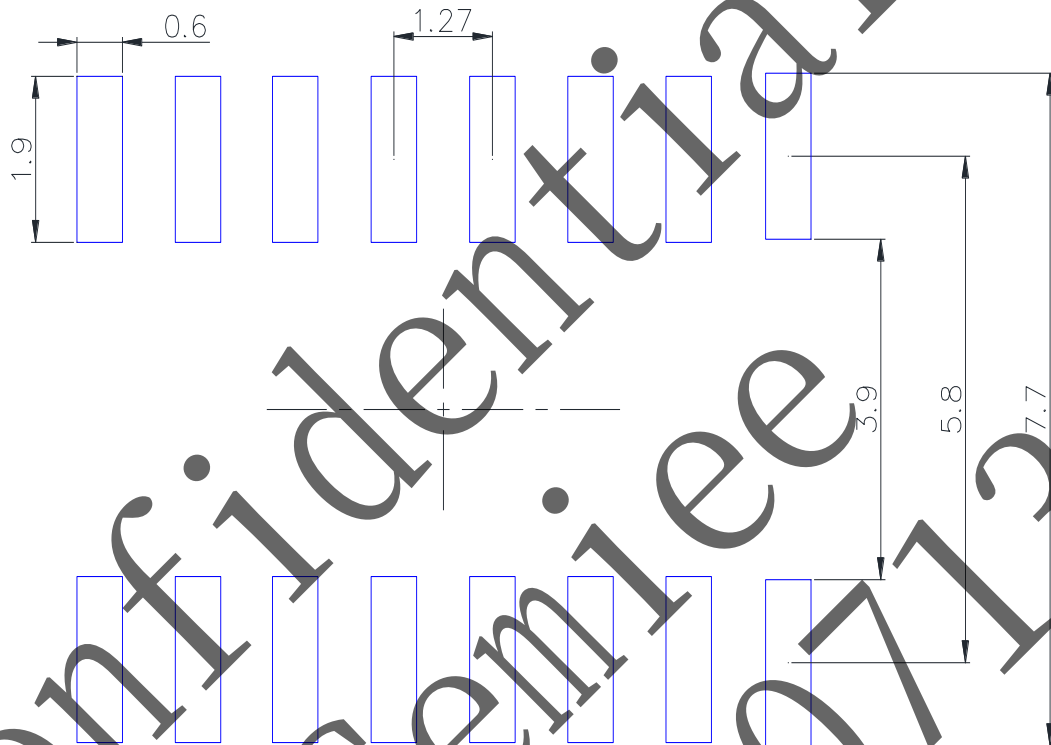


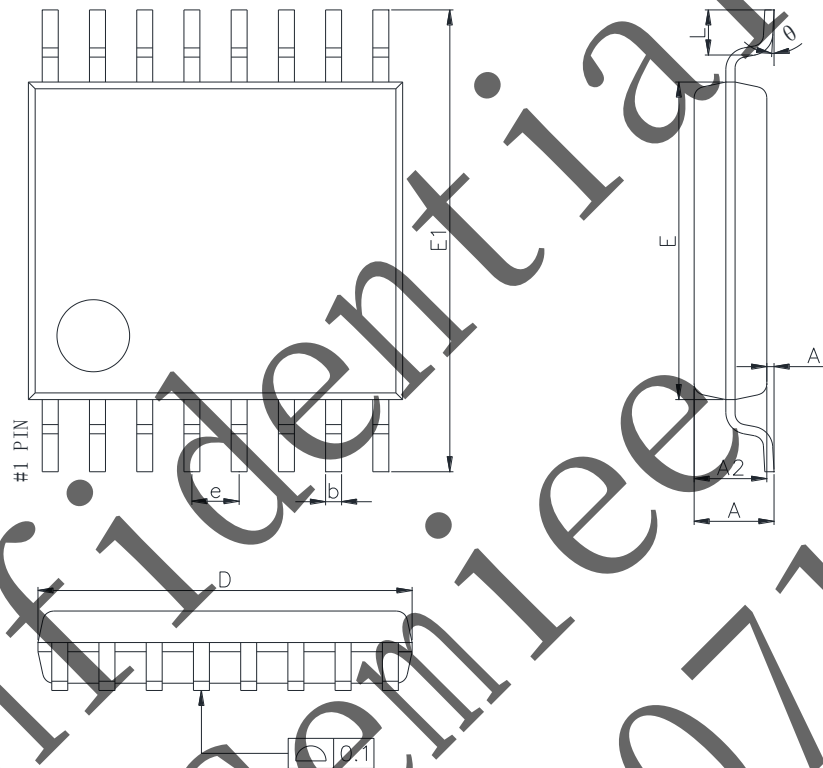
Figure 13. Read control register

**Package Outline Dimensions (SOP-16)**
**SOP-16      Unit (mm)**


| Symbol | Dimensions in Millimeters |        | Dimensions in Inches |       |
|--------|---------------------------|--------|----------------------|-------|
|        | Min.                      | Max.   | Min.                 | Max.  |
| A      | 1.300                     | 1.750  | 0.051                | 0.069 |
| A1     | 0.100                     | 0.250  | 0.004                | 0.010 |
| A2     | 1.400                     | 1.500  | 0.055                | 0.059 |
| b      | 0.33                      | 0.51   | 0.013                | 0.020 |
| c      | 0.17                      | 0.250  | 0.007                | 0.010 |
| D      | 9.800                     | 10.000 | 0.386                | 0.394 |
| E      | 3.800                     | 4.000  | 0.150                | 0.157 |
| E1     | 5.800                     | 6.200  | 0.228                | 0.244 |
| e      | 1.270 (BSC)               |        | 0.050 (BSC)          |       |
| L      | 0.400                     | 1.270  | 0.016                | 0.050 |
| θ      | 0°                        |        | 8°                   |       |

**Recommend Land Pattern Layout (SOP-16)**
**SOP-16**
**Unit (mm)**

**Note:**

1. All dimensions are in millimeter
2. Recommend tolerance is within  $\pm 0.1\text{mm}$
3. Change without notice

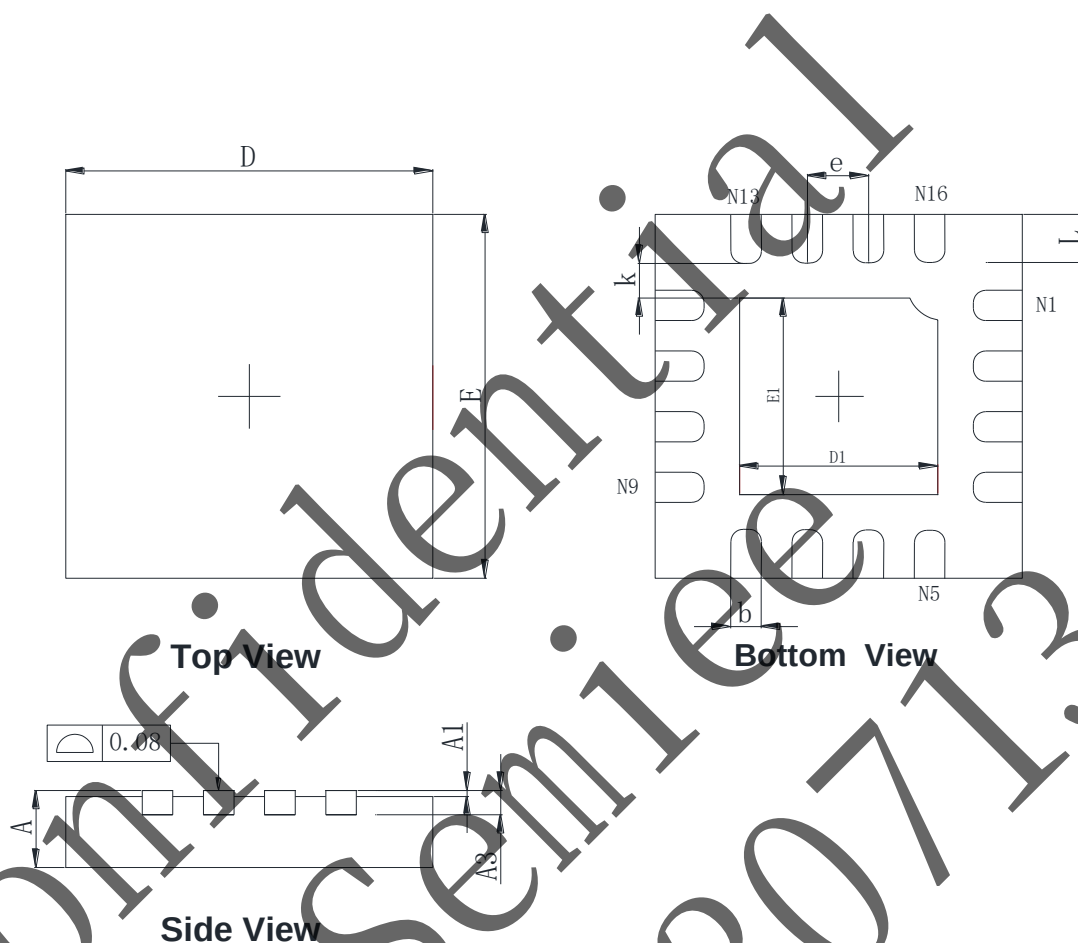
**Package Outline Dimensions (TSSOP-16)**
**TSSOP-16      Unit (mm)**


| Symbol | Dimensions in Millimeters |       | Dimensions in Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min.                      | Max.  | Min.                 | Max.  |
| A      |                           | 1.200 |                      | 0.047 |
| A1     | 0.050                     | 0.150 | 0.002                | 0.006 |
| A2     | 0.800                     | 1.000 | 0.031                | 0.039 |
| b      | 0.190                     | 0.300 | 0.007                | 0.012 |
| c      | 0.090                     | 0.200 | 0.004                | 0.008 |
| D      | 4.900                     | 5.100 | 0.193                | 0.201 |
| E      | 4.300                     | 4.500 | 0.169                | 0.177 |
| E1     | 6.200                     | 6.600 | 0.244                | 0.260 |
| e      | 0.650 (BSC)               |       | 0.026 (BSC)          |       |
| L      | 0.400                     | 0.800 | 0.016                | 0.031 |
| θ      | 0°                        | 8°    | 0°                   | 8°    |

**Recommend Land Pattern Layout (TSSOP-16)**
**TSSOP-16**
**Unit (mm)**

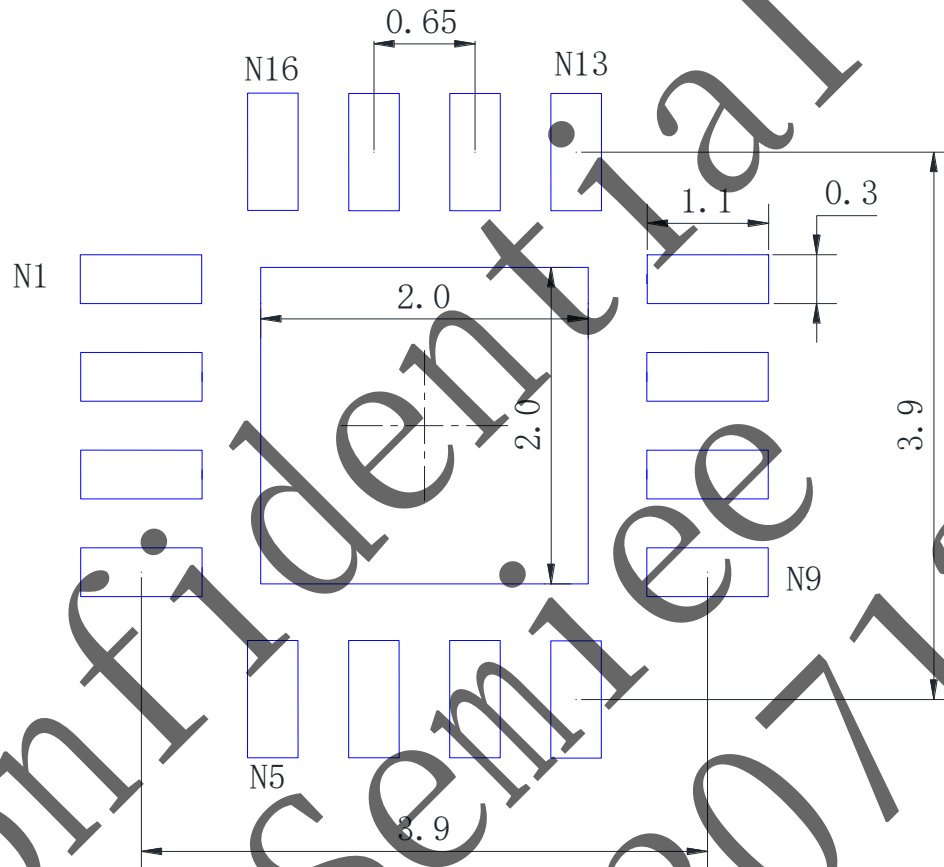
**Note:**

1. All dimensions are in millimeter
2. Recommend tolerance is within  $\pm 0.1\text{mm}$
3. Change without notice

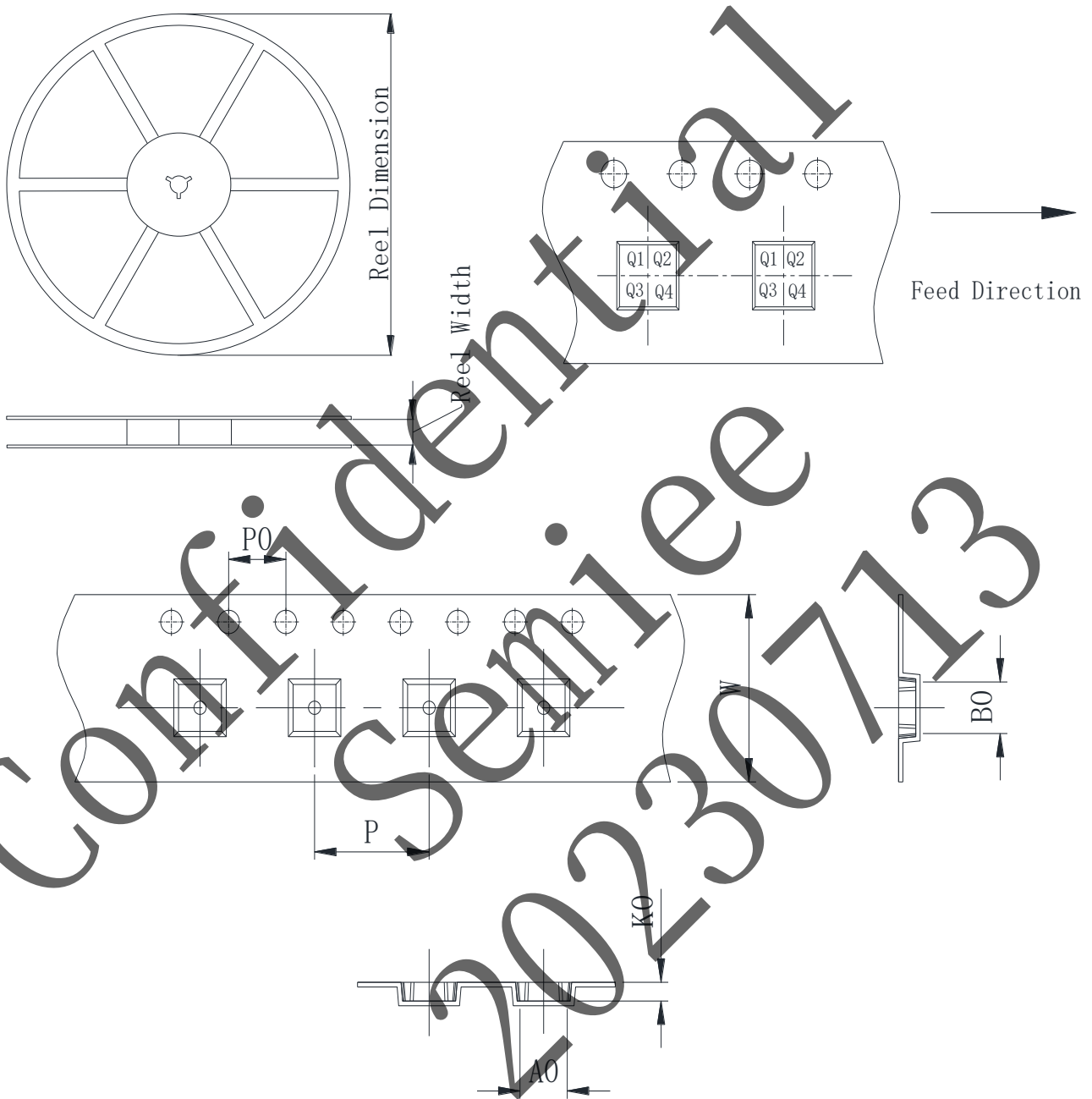
**Package Outline Dimensions (QFN4x4-16)**
**QFN4x4-16 Unit (mm)**


| Symbol | Dimensions in Millimeters |       | Dimensions in Inches |       |
|--------|---------------------------|-------|----------------------|-------|
|        | Min.                      | Max.  | Min.                 | Max.  |
| A      | 0.700                     | 0.800 | 0.028                | 0.031 |
| A1     | 0.000                     | 0.050 | 0.000                | 0.002 |
| A3     | 0.203REF.                 |       | 0.008REF             |       |
| D      | 3.900                     | 4.100 | 0.154                | 0.161 |
| E      | 3.900                     | 4.100 | 0.154                | 0.161 |
| D1     | 2.000                     | 2.200 | 0.079                | 0.087 |
| E1     | 2.000                     | 2.200 | 0.079                | 0.087 |
| k      | 0.200MIN.                 |       | 0.008REF             |       |
| b      | 0.250                     | 0.350 | 0.010                | 0.014 |
| e      | 0.650TYP.                 |       | 0.026TYP             |       |
| L      | 0.450                     | 0.650 | 0.018                | 0.026 |

Note: pin 1 shape for thermal pad on backside is not limited to bevel, it can be a notch or arch

**Recommend Land Pattern Layout (QFN4x4-16)**
**QFN4x4-16 Unit (mm)**

**Note:**

1. All dimensions are in millimeter
2. Recommend tolerance is within  $\pm 0.1\text{mm}$
3. Change without notice

**Packing information**


| Package type | Reel size | Reel dimension (±3.0mm) | Reel width (±1.0mm) | A0 (±0.1mm) | B0 (±0.1mm) | K0 (±0.1mm) | P (±0.1mm) | P0 (±0.1mm) | W (±0.3mm) | Pin1 |
|--------------|-----------|-------------------------|---------------------|-------------|-------------|-------------|------------|-------------|------------|------|
| SOP16        | 13'       | 330                     | 16.8                | 6.5         | 10.3        | 2.1         | 8.0        | 4.0         | 16.0       | Q1   |
| TSSOP-16     | 13'       | 330                     | 12.8                | 6.8         | 5.4         | 1.2         | 8.0        | 4.0         | 12.0       | Q1   |
| QFN4x4-16    | 13'       | 330                     | 12.8                | 4.3         | 4.3         | 1.1         | 8.0        | 4.0         | 12.0       | Q2   |

Low Voltage 4-Channel I<sup>2</sup>C/SMBus Switch with Reset

## Revision History

| Version | Date    | Change Content                    |
|---------|---------|-----------------------------------|
| Ver1.0  | 2020/12 | Initial Version                   |
| Ver1.1  | 2021/01 | Update Ordering Information       |
| Ver1.2  | 2021/07 | Update Slave Address              |
| Ver1.3  | 2022/04 | Update Electrical Characteristics |

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