TPS61178x 20-V, 10-A Fully-Integrated Synchronous Boost with Load Disconnect Control

1 Features

- Input Voltage Range: 2.7 V to 20 V
- Output Voltage Range: 4.5 V to 20 V
- Programmable Switch Peak Current: up to 10 A
- Two 16-mΩ FETs Integrated
- Efficiency up to 96%: V_{IN} = 7.2 V, V_{OUT} = 16 V, I_{OUT} = 2 A
- Adjustable Switching Frequency: up to 2.2 MHz
- External Clock Synchronization: 200 kHz to 2.2 MHz
- Gate Driver for Load Disconnect
- Hiccup Short Protection
- Over Voltage Protection
- Auto PFM Operation - TPS61178
- Forced PWM Mode - TPS611781
- 3.0-mm x 3.5-mm 13-pin VQFN Hotrod Package
- Create a Custom Design Using the TPS61178 With the WEBENCH® Power Designer

2 Applications

- Portable Speaker
- Source Driver of LCD Display
- Supply for the Power Amplifier
- Supply for the Motor Driver
- USB Type-C Power Delivery

3 Description

The TPS61178x family is a 20-V synchronous Boost converter with the gate driver built-in for load disconnect. The TPS61178x integrates two low on-resistance power FETs: A 16-mΩ switching FET and a 16-mΩ rectifier FET.

The TPS61178x uses the fixed frequency peak current mode control with the slope compensation integrated. At the light load, the TPS61178 enters into the auto PFM mode while TPS611781 is in the forced PWM mode.

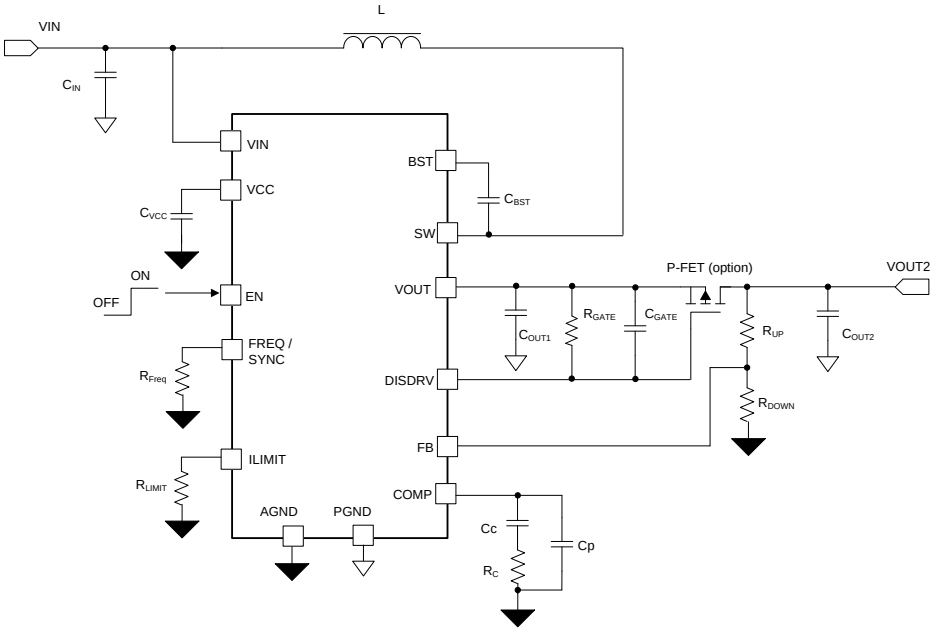
The TPS61178x could isolate the output from input side when shutdown. Once the output is shorted, it enters into the hiccup mode to lower the thermal stress and can recover automatically after the short releases. Additionally, the TPS61178x also has OVP and thermal protection to avoid the fault operation. The TPS61178x is in a 3.0-mm x 3.5-mm 13-pin VQFN package with enhanced thermal dissipation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61178	QFN (13)	3.00 mm × 3.5 mm
TPS611781		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2019) to Revision E — **Page**

- Restored hyperlink cross reference at the Thermal Information table footnote. ... 4
- Deleted right-hand column (A/B/S) in the Electrical Characteristics table. ... 5

Changes from Revision C (March 2018) to Revision D — **Page**

- Corrected term 1–DR to 1–D in Equation 21 ... 23

Changes from Revision B (September 2017) to Revision C — **Page**

- Changed Equation 21 ... 23

Changes from Revision A (April 2017) to Revision B — **Page**

- Changed graphs for Figure 1 through Figure 6 to include 3-A load ... 7

Changes from Original (February 2017) to Revision A — **Page**

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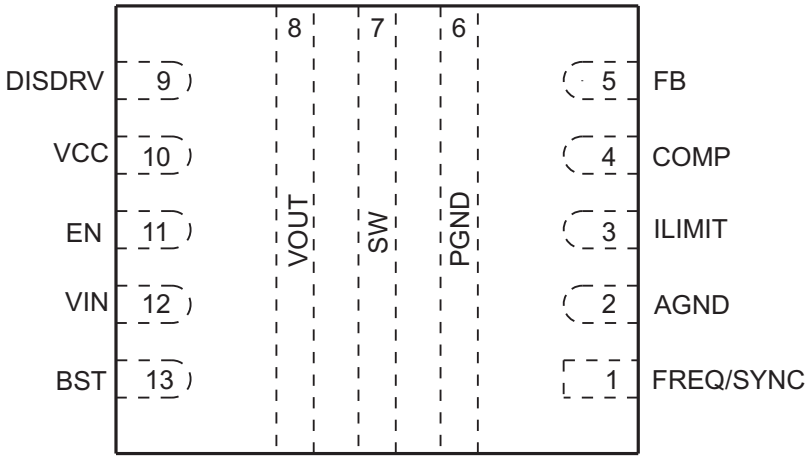
5 Device Comparison Table

Part Number	Operation Mode at Light Load
TPS61178	Auto PFM
TPS611781	Forced PWM

6 Pin Configuration and Functions

(RNW)
(13-Pin QFN)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
FREQ / SYNC	1	I	The switching frequency is programmed by a resistor between this pin and the AGND. The internal oscillator can be synchronized by an external clock connecting into this pin. This pin can not be float in application.
AGND	2	-	Analog signal ground of the IC. Connect the AGND to PGND via a single point on the printed circuit board.
ILIMIT	3	I	Programming the switching peak current limit by a resistor between this pin and AGND.
COMP	4	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and AGND.
FB	5	I	Output voltage feedback, a resistor divider connecting to this pin sets the output voltage.
PGND	6	PWR	Power ground
SW	7	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power FET and the source of the internal high-side power FET.
VOUT	8	PWR	Boost converter output
DISDRV	9	O	A gate drive output for the external disconnect FET. Connect the DISDRV pin to the gate of the external FET. Leave it floating if not using the load disconnect function.
VCC	10	O	Output of the internal regulator. A ceramic capacitor of more than 1.0 µF is required between this pin and ground
EN	11	I	Enable logic input. Logic high level enables the device and low level shutdown the device.
VIN	12	I	IC power supply input.
BST	13	O	Power supply for high-side FET gate driver. A capacitor must be connected between this pin and the SW pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage range at terminals [2]	BST	–0.3	SW + 7	V
	VIN, SW, VOUT, DISCRG, EN	–0.3	23	V
	VCC, FB, COMP, FREQ / SYNC, ILIMIT	–0.3	7	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ [1] Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[2]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[3]	±750	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		20	V
V_{OUT}	Outputvoltage	4.5		20	V
L	Effective inductance range	0.47	3.3		µH
R_{FB}	Feedback resistance (low side)			200	kΩ
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS61178 RNR (QFN Package) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report..

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7.5 Electrical Characteristics

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

			MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		20	V
V_{IN_UVLO}	Input voltage under voltage lockout (UVLO) threshold	V_{IN} rising		2.6	2.7	V
		V_{IN} falling		2.2	2.3	
V_{IN_HYS}	VIN UVLO hysteresis			400		mV
V_{CC}	VCC regulation voltage	ICC = 5mA, VIN = 8V		6		V
V_{CC_UVLO}	VCC UVLO threshold	VCC falling		2.1		V
I_Q (TPS61178)	Quiescent current into V_{IN} pin	IC enabled, no load, no ext. FET V_{IN} = 6 V, V_{OUT} = 20 V, V_{FB} = 1.3 V, T_J up to 85 ºC		1.5	3	µA
	Quiescent current into V_{IN} pin	IC enabled, no load, no ext. FET V_{IN} = 20 V, V_{OUT} = 20 V, V_{FB} = 1.3 V,T_J up to 85 ºC		270	320	µA
	Quiescent current into V_{OUT} pin	IC enabled, no load, no ext. FET V_{IN} = 6 V, V_{FB} = 1.3 V, V_{OUT} = 20 V, T_J up to 85 ºC		250	300	µA
	Quiescent current into V_{OUT} pin	IC enabled, no load, no ext. FET V_{IN} = 20 V, V_{OUT} = 20 V, V_{FB} = 1.3 V, T_J up to 85 ºC		5	12	µA
I_{SD}	Shutdown current into V_{IN} pin	IC disabled, V_{IN} = 6 V, –40 °C ≤ T_J ≤ 85°C		1	3.5	µA
		IC disabled, VIN = 20 V, –40 °C ≤ T_J ≤ 85°C		3	6	µA
I_{LS_LKG}	Reverse leakage current into SW	IC disabled, VIN = V_{OUT} = SW = 20 V –40 °C ≤ T_J ≤ 85°C		0.1	6.5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage range	Freq = 500kHz	4.5		20	V
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 8 V, V_{OUT} rising	20.5	21	21.5	V
POWER SWITCHES						
$R_{DS(on)}$	High-side MOSFET on resistance	V_{CC} = 6 V		16	25	mΩ
	Low-side MOSFET on resistance	V_{CC} = 6 V		16	25	mΩ
Gm	Power stage trans-conductance (peak current ratio with comp voltage)	V_{CC} = 6 V		12		A/V
CURRENT LIMIT						
I_{LIM_SW}	TPS61178	R_{LIMIT} = 80.6 kΩ	6.4	8	9.4	A
I_{LIM_SW}	TPS611781	R_{LIMIT} = 80.6 kΩ	5.7	7.4	8.7	A
I_{LIM_SHORT}	TPS61178 short current limit			20		A
VOLTAGE REFERNCE						
V_{REF}	Reference Voltage at FB pin	PWM mode	1.180	1.198	1.210	V
		PFM mode		101%		V_{REF}
I_{FB_LKG}	Leakage current into FB pin			10	60	nA
EN / SYNC LOGIC						
V_{EN_H}	EN Logic high threshold				1.2	V
V_{EN_L}	EN Logic Low threshold		0.4			V

Electrical Characteristics (continued)

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

			MIN	TYP	MAX	UNIT
R_{EN}	EN pulldown resistor			800		kΩ
V_{SYNC_H}	SYNC clock high threshold				1.2	V
V_{SYNC_L}	SYNC clock low threshold		0.4			V
ERROR AMPLIFIER						
V_{COMPH}	COMP output high voltage	High threshold, V_{FB} = V_{REF} - 200 mV		1.9		V
V_{COMPL}	COMP output low voltage	Low threshold, V_{FB} = V_{REF} + 200 mV		1.25		V
G_{mEA}	Error amplifier trans conductance	V_{COMP} = 1.5 V		195		uS
I_{SINK}	Comp pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1.5 V		20		uA
I_{SOURCE}	Comp pin source current	V_{FB} = V_{REF} –200 mV, V_{COMP} = 1.5 V		20		uA

7.6 Timing Requirements

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

			MIN	TYP	MAX	UNIT
CURRENT LIMIT						
t_{SHORT_ON}	Short active time			4		ms
t_{SHORT_OFF}	Time for Auto retry protection off time			90		ms
SOFT START						
$t_{STARTUP}$	Startup time	V_{IN} = 8 V, V_{OUT} = 16 V		3.2		ms
t_{PRE_CHARG}	Pre charge time	Pre charge time	1.8	2.6	3.4	ms
PROTECTION						
t_{SD_R}	Thermal shutdown rising threshold	TJ rising		150		°C
t_{SD_F}	Thermal shutdown falling threshold	TJ falling		130		°C

7.7 Switching Characteristics

over operating free-air temperature range, V_{IN} = 2.7 V to 14 V and V_{OUT} = 16 V, V_{CC} = 6 V, R_{LIMIT} = 80.6 kΩ. Typical values are at T_J = 25°C, (unless otherwise noted)

			MIN	TYP	MAX	Unit
SWITCHING FREQUENCY / SYNC						
f_{SW}	Switching frequency	R_{FREQ} = 342 kΩ	400	500	600	kHz
		R_{FREQ} = 842 kΩ	160	200	240	kHz
		R_{FREQ} = 75 kΩ	1900	2200	2500	kHz
t_{ON_min}	Minimum on time			105	135	ns
t_{OFF_min}	Minimum off time			140	180	ns
f_{SYNC_MIN}	Min Frequency using external clock		190	200	210	kHz
f_{SYNC_MAX}	Max Frequency using external clock		2090	2200	2310	kHz
GATE DRIVER FOR LOAD DISCONNECT						
I_{GH_SINK}	External PFET drive current			55		uA

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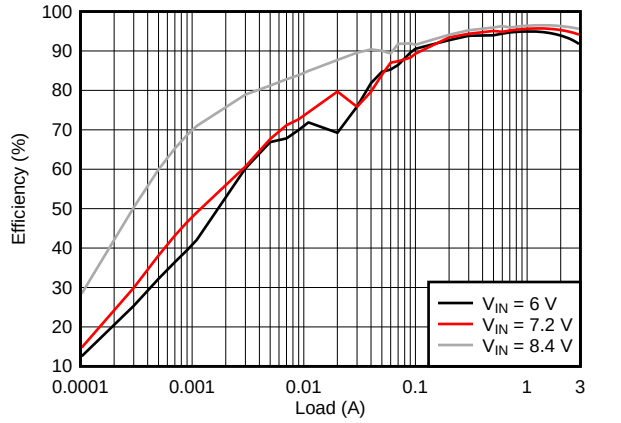
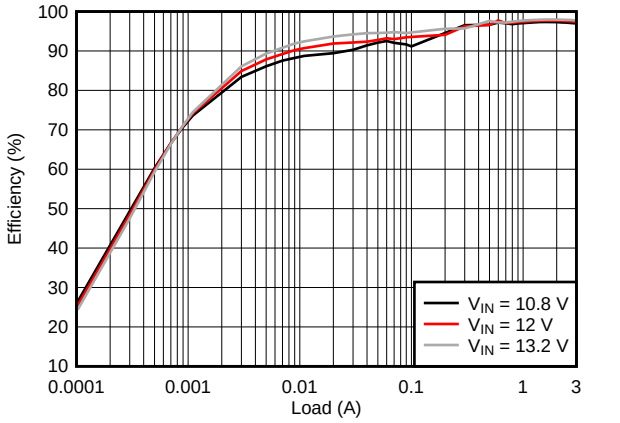
7.8 Typical Characteristics



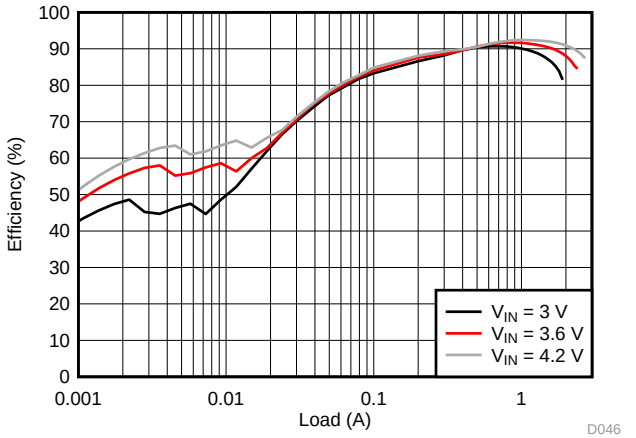
V_{OUT} = 16 V L = 3.3 µH Auto PFM

Figure 1. Efficiency vs. Output Current



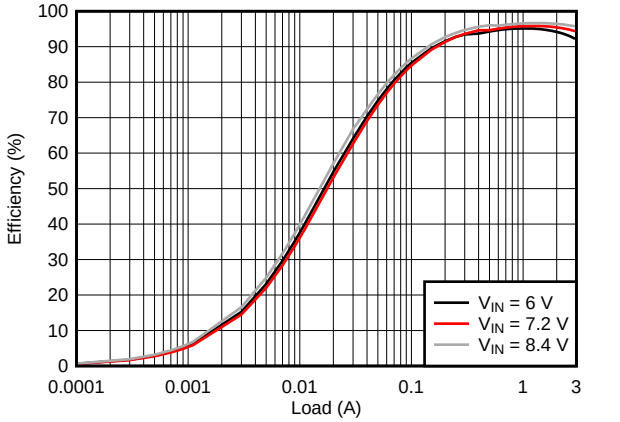
V_{OUT} = 16 V L = 3.3 µH Auto PFM

Figure 2. Efficiency vs. Output Current



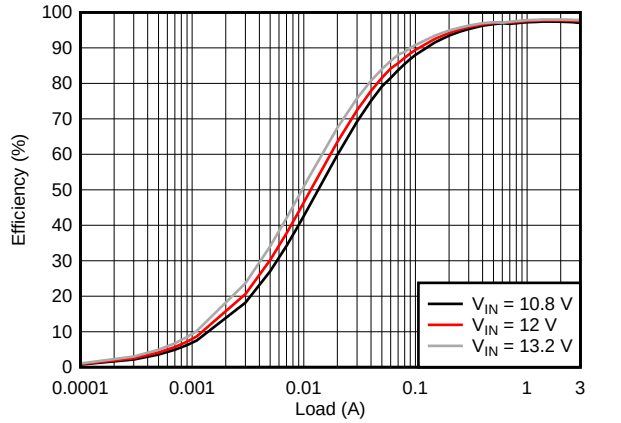
V_{OUT} = 14 V L = 1.8 µH Auto PFM

Figure 3. Efficiency vs. Output Current



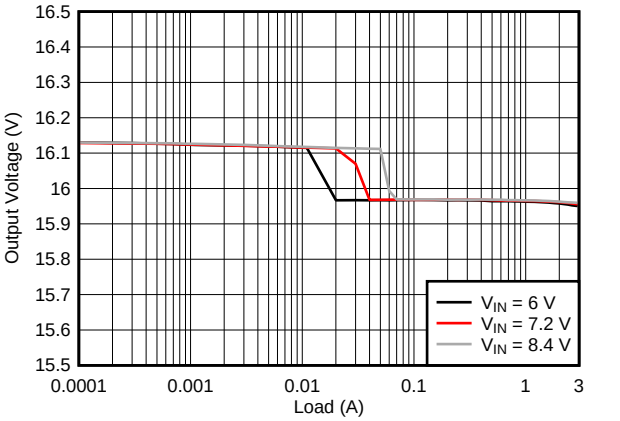
V_{OUT} = 16 V L = 3.3 µH Forced PWM

Figure 4. Efficiency vs. Output Current



V_{OUT} = 16 V L = 3.3 µH Forced PWM

Figure 5. Efficiency vs. Output Current



V_{OUT} = 16 V L = 3.3 µH Auto PFM

Figure 6. Output Voltage vs. Load

Typical Characteristics (continued)

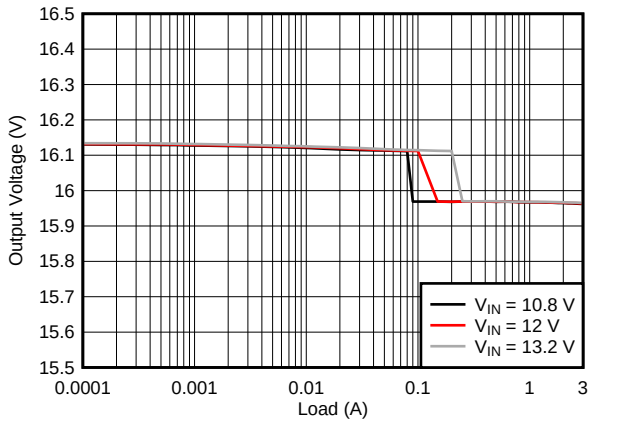


Figure 7. Output Voltage vs. Load

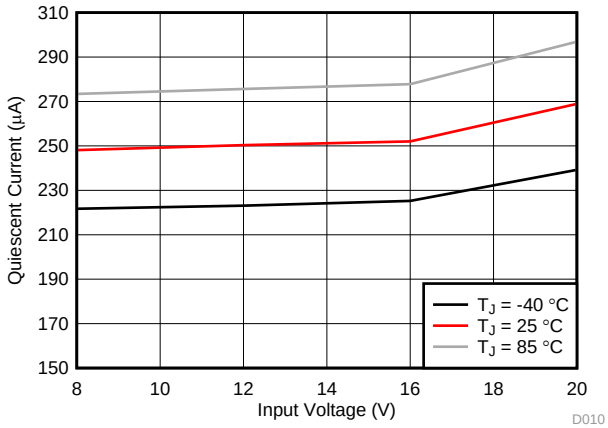


Figure 8. Quiescent Current vs V_{IN}

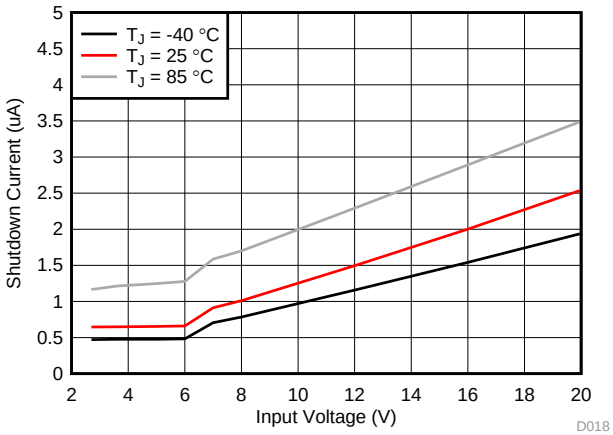


Figure 9. Shutdown Current vs V_{IN}

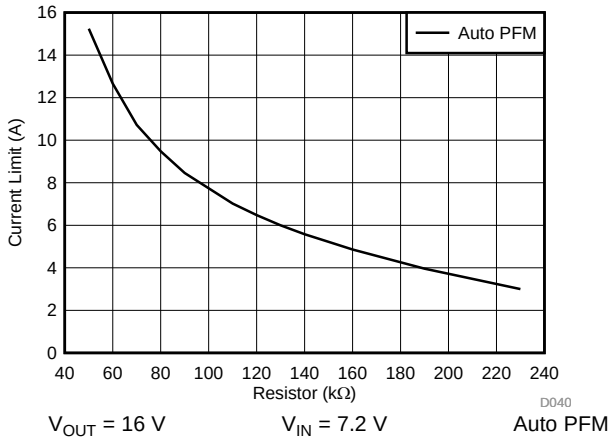


Figure 10. Switch Current Limit vs Setting Resistor

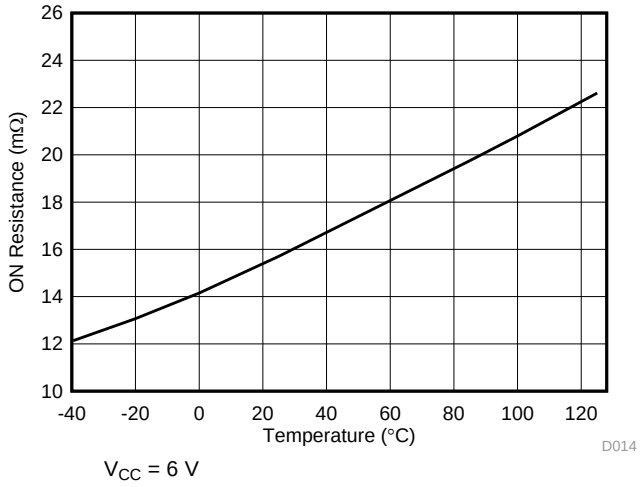


Figure 11. LS Rdson vs Temperature

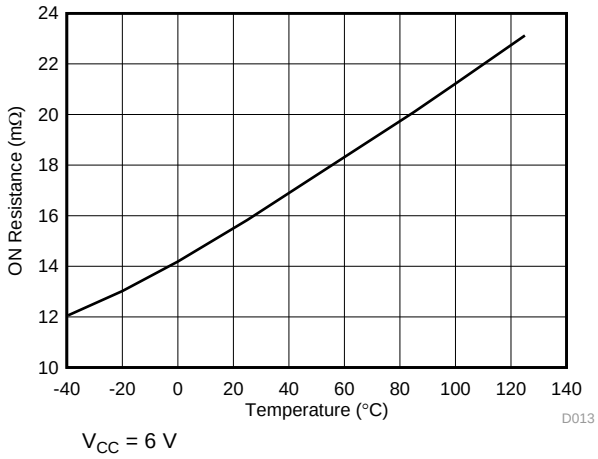


Figure 12. HS Rdson vs Temperature

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Typical Characteristics (continued)

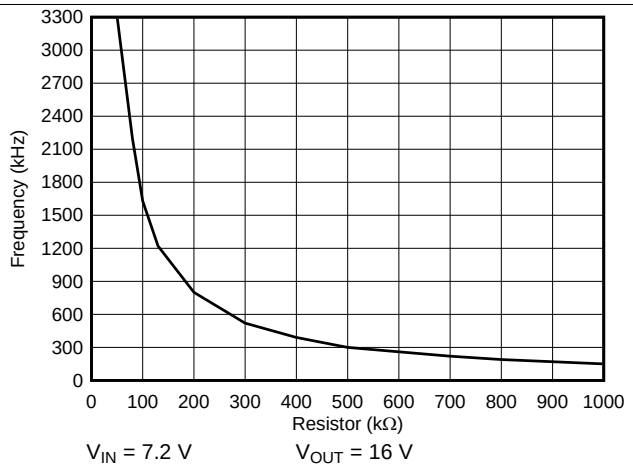


Figure 13. Frequency vs Setting Resistor

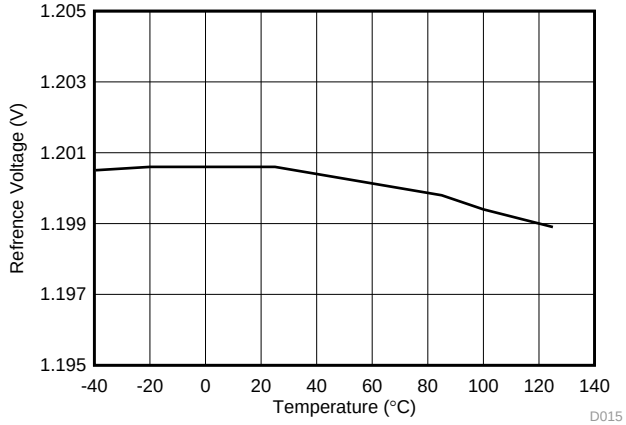


Figure 14. Reference Voltage vs Temperature

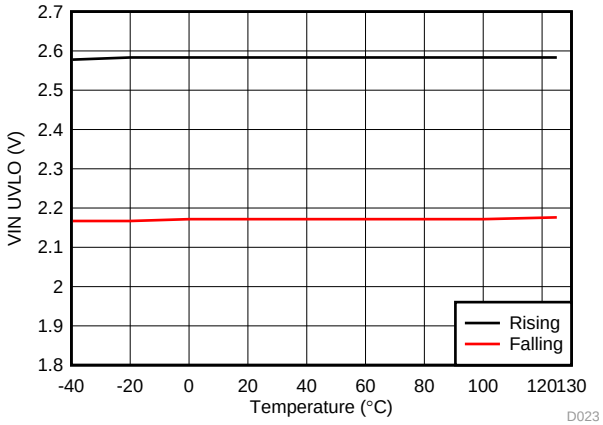


Figure 15. V_{IN} UVLO Rising / Falling vs Temperature

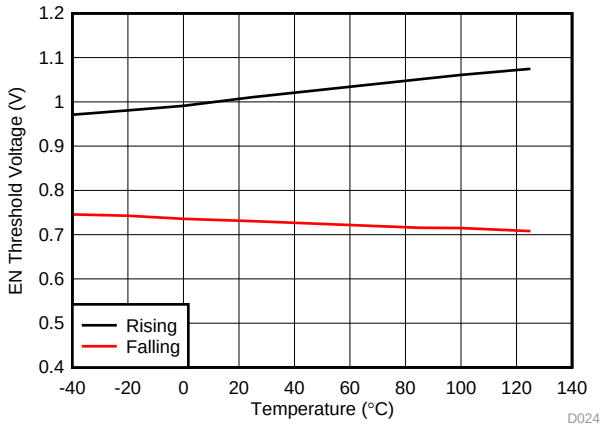


Figure 16. EN Threshold Rising / Falling vs Temperature

8 Detailed Description

8.1 Overview

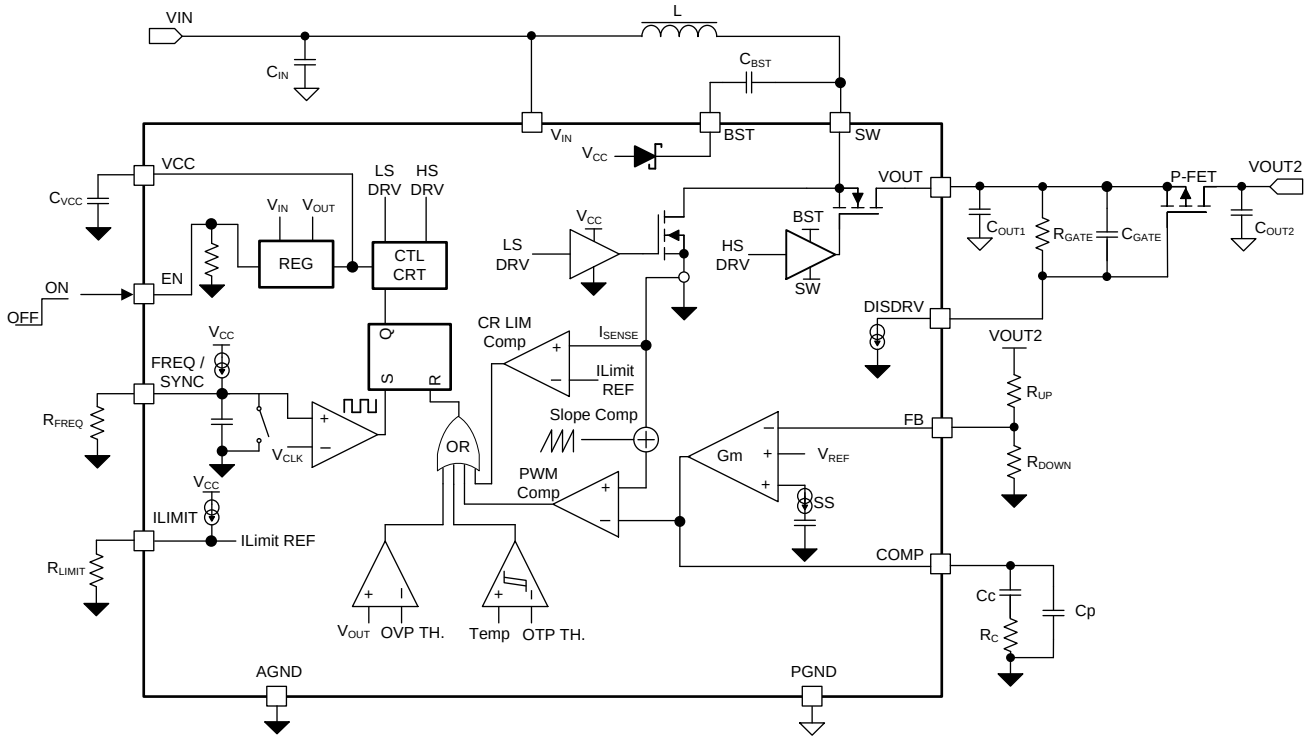
The TPS61178x family is a synchronous boost converter designed for delivering the switch peak current up to 10 A and output voltage reaching to 20 V. The TPS61178x family operates at a fixed frequency pulse-width modulation (PWM) at the moderate to heavy load currents. At the light load current, the TPS61178 operates in the PFM mode while the TPS611781 operates in the Forced PWM mode. The PFM mode brings the high efficiency crossing the entire load range while the Forced PWM mode can avoid the noise interference at the light load.

With the peak current mode control scheme, the TPS61178x provides the excellent line and load transient response with the minimal output capacitance. The external loop compensation brings the flexibility to use a wider range of the inductor and output capacitor combinations.

The TPS61178x supports the adjustable switching frequency up to 2.2 MHz. The device implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. Additionally, if the output current further increases and exceeds the short current threshold or the output voltage drops below the short threshold. The TPS61178x triggers the hiccup short protection and recovers automatically once the short condition releases.

Additionally, the TPS61178x provides the gate driver for the external FET to isolate the output from input end during shutdown.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Under-voltage Lockout

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.3 V. A hysteresis of 400 mV is added so that the device cannot be enabled again until the input voltage exceeds 2.7 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.3 V and 2.7 V.

8.3.2 Enable and Disable

When the input voltage is above UVLO rising threshold of 2.7 V and the EN pin is pulled high above 1.2 V, the TPS61178X is enabled. When the EN pin is pulled below 0.4 V, the TPS61178x goes into the shutdown mode and stops switching.

8.3.3 Startup

When the input voltage to the device exceeds the UVLO threshold and EN pin pulled to high as well, the TPS61178x starts to ramp up the output voltage. There is a switching pre-charge phase and the output voltage is charged up to 10% higher than the input voltage (1.1 x V_{IN}). The switching frequency is a fixed 500 kHz at the pre-charge phase.

After the pre-charge phase ends (typical 2.6 ms), The TPS61178x regulates the FB pin to the internal soft start voltage and results in a gradual rise of the output voltage starting from the input voltage level to the target output voltage. The soft start time is typical 3.2 ms, which helps the regulator to gradually reach the steady state setting point, thus reducing the startup stresses and surges. The switching frequency follows the oscillator setting by the resistor connecting with the FREQ / SYNC pin.

If the device is synchronized by the external clock, the switching frequency is fixed 500 kHz at the soft start phase and changes to the external clock when the soft start phase ends.

8.3.4 Load Disconnect Gate Driver

The TPS61178 device provides a DISDRV pin to drive the external FET at the output side, which completely disconnects the output from the input end during shutdown or output short happens. During the device's start-up phase, the disconnect FET is controlled by the gate driver voltage of the external disconnect FET, there is an internal 55 µA (typical) sink current. The load disconnect FET connection is shown as *Figure 17*

The driver voltage and turn on / off timing can be set via the resistor and capacitor connecting between with the DISDRV pin and the source of the external FET. See the Application and Implementation section for the details of how to select the gate resistor and capacitor

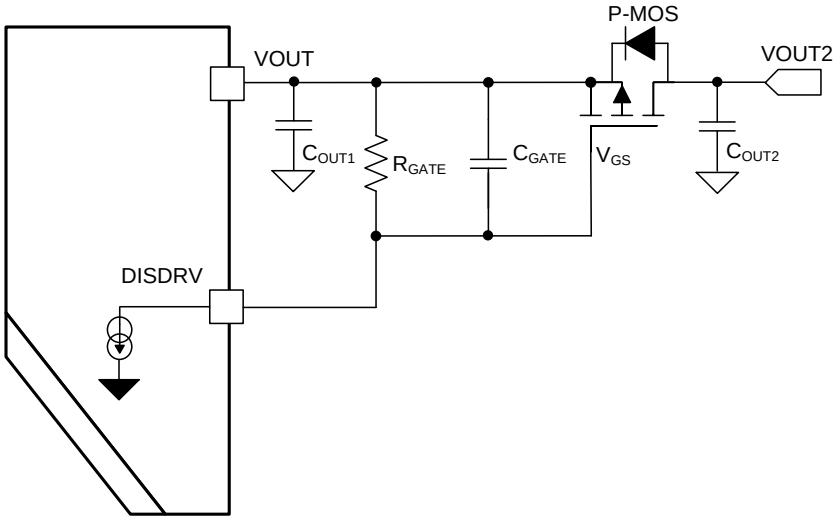

Figure 17. The Load Disconnect FET Connected

Feature Description (continued)

8.3.5 Adjustable Peak Current Limit

When the TPS61178x is in the normal boost switching phase, the device is prevented from the over current condition via the cycle by cycle current limit by sensing the current through the internal low-side FET. When the peak switch current triggers the current limit threshold, the low-side switch turns off to prevent the switching current further increasing.

The peak switch current limit can be set by a resistor connecting with the I_{LIMIT} pin. The relationship between the current limit and the resistor is determined by Equation 1

$$R_{LIMIT} = \frac{745}{I_{LIMIT}} \tag{1}$$

Where R_{LIMIT} is the resistor for setting the current limit, with the unit of kΩ, I_{LIMIT} is switching peak current limit, the unit is A. For instance, when the resistor value is 50 kΩ, the switch peak current limit is 15 A.

Figure 18 shows the current limit versus the setting resistor for both TPS61178 (Auto PFM) and TPS611781 (Forced PWM) with 7.2-V input to 16-V output.

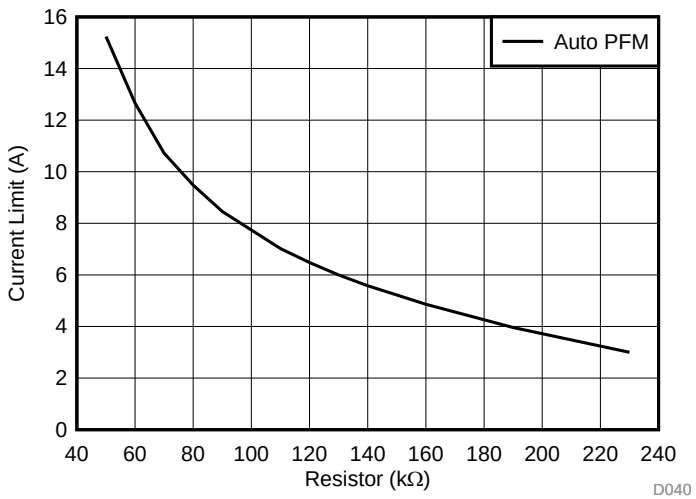

Figure 18. Switch Current Limit vs. Setting Resistor

The current limit value varies with the duty cycle, Figure 30 shows the bench measurement current limit at different duty cycles at R_{LIMIT} = 80.6 kΩ.

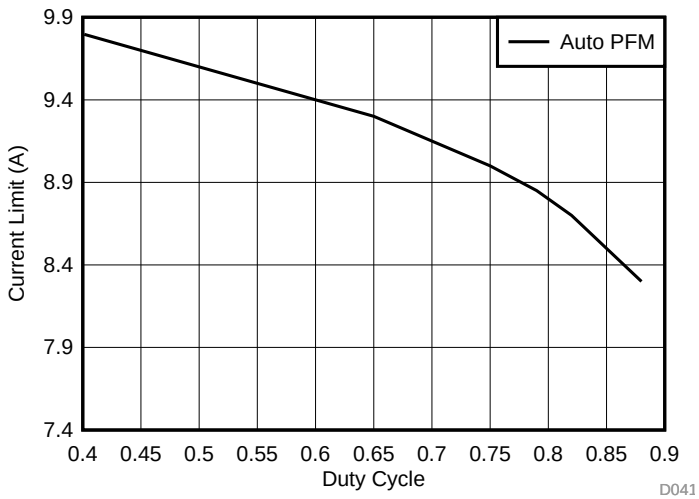

Figure 19. Switch Current Limit vs. Duty Cycle

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Feature Description (continued)

For the TPS611781, which works in the Forced PWM mode at the light load, the current limit is typically 0.8 A lower than TPS61178 (Auto PFM) with the same setting resistor.

8.3.6 Output Short Protection (with load disconnected FET)

In addition to the cycle-by-cycle current limiting, the TPS61178x also has the output short protection. If the inductor current reaches the short protection limit threshold (typical 20A) or the output voltage drops below 30% (typical) of the normal output voltage, the device enters into the hiccup protection mode. In the hiccup mode, the device shuts down itself and restarts after 90ms (typical) waiting time which helps to reduce the total thermal dissipation. After the short condition releases, the device can recover automatically and restart the start-up phase. The hiccup protection scheme is illustrated in Figure 20.

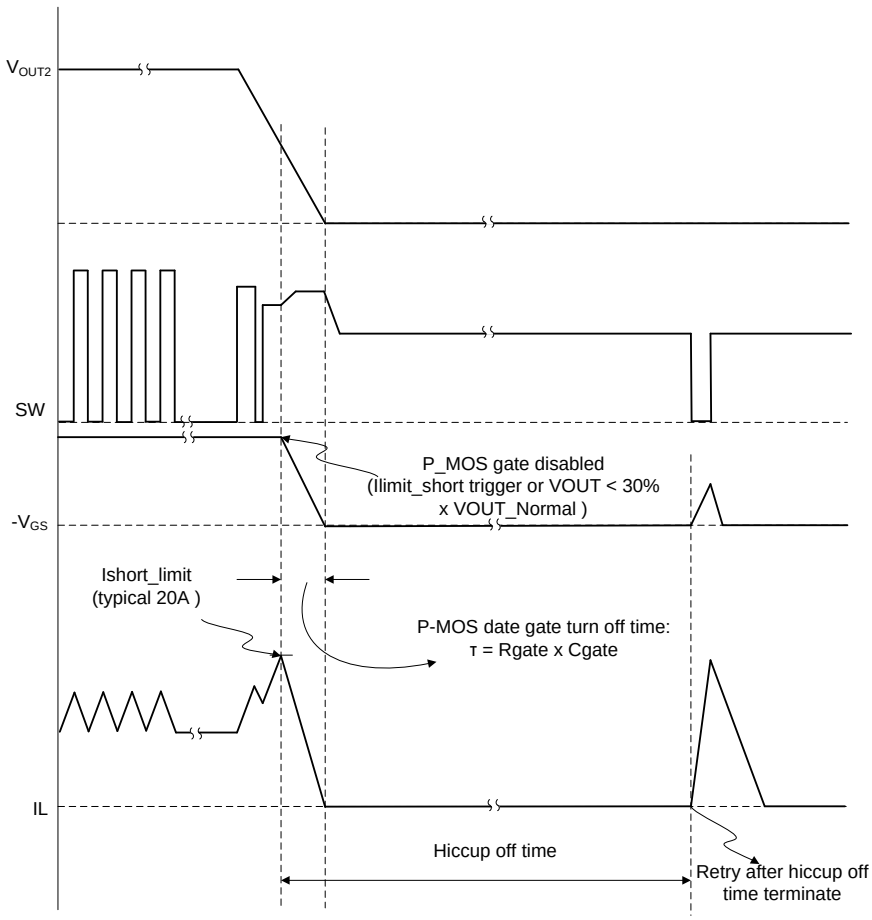

Figure 20. Output Short Protection

8.3.7 Adjustable Switching Frequency

The TPS61178x features of a wide adjustable switching frequency ranging up to 2.2 MHz. The switching frequency is set by a resistor connecting with the FREQ / SYNC pin. This pin cannot be left floating in the application. Use Equation 2 and Equation 3 to calculate the resistor value for a desired frequency.

$$T = \frac{1}{Freq} = k \times C_{FREQ} \times R_{FREQ} + T_{DELAY} \tag{2}$$

$$R_{FREQ} = \frac{\frac{1}{Freq} - T_{DELAY}}{k \times C_{FREQ}}$$

where

Feature Description (continued)

- T_{DELAY} = 50 nS, k = 3, C_{FREQ} = 1.8 pF (3)

For instance, if the R_{FREQ} is 342 kΩ, the frequency is 500 kHz.

Figure 21 shows the switching frequency versus the setting resistor, which is measured with V_{OUT} = 16 V from V_{IN} = 7.2 V .

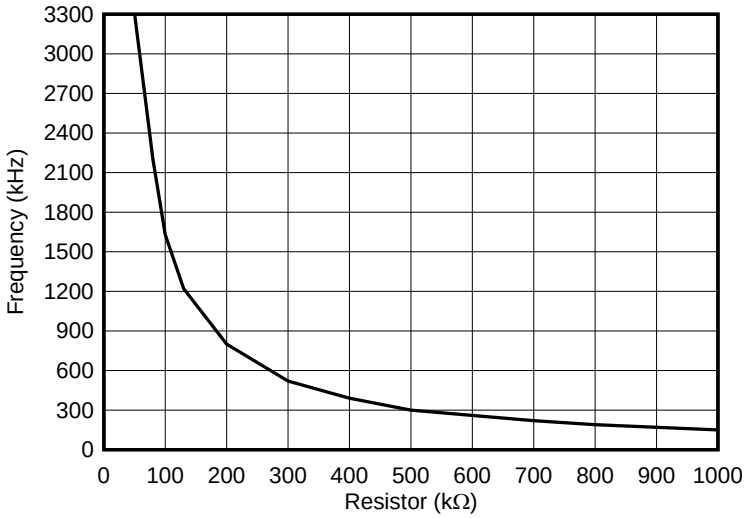

Figure 21. Switching Frequency vs Setting Resistor

8.3.8 External Clock Synchronization (TPS611781)

The FREQ/ SYNC pin can be used to synchronize the internal oscillator by an external clock. A positive voltage at the FREQ / SYNC pin must exceed the rising threshold (1.2 V) while must be lower than the falling threshold (0.4 V) to trip the internal synchronization pulse detector. The recommended frequency for the external clock is between 200 kHz and 2.2 MHz.

8.3.9 Error Amplifier

The TPS61178x has a trans-conductance amplifier and compares the feedback voltage with the internal voltage reference (or the internal soft start voltage during startup phase). The trans-conductance of the error amplifier is 195 µA / V typically. The loop compensation components are required to be placed between the COMP terminal and ground to balance the loop stability and the transient response time.

8.3.10 Slope Compensation

The TPS61178x adopts the peak current mode control and adds a compensating ramp to the switch current signal. This slope compensation prevents the sub-harmonic oscillations when the duty cycle is larger than 50%. The available peak inductor current varies a little bit with operating duty cycles shown in Figure 19.

8.3.11 Start-up with the Output Pre-Biased

The TPS61178x has been designed to prevent the low-side FET from discharging a pre-biased output. During the pre-biased startup, both high-side and low-side FETs are not allowed to be turned on until the internal soft start voltage is higher than the sensed output voltage at FB pin.

8.3.12 Bootstrap Voltage (BST)

The TPS61178x has an integrated bootstrap regulator, and requires a small ceramic capacitor between the BST pin and SW pin to provide the gate drive voltage for the high-side FET. The bootstrap capacitor is charged when the BST-SW voltage is below regulation. The value of this ceramic capacitor should be above 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and DC biased voltage.

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Feature Description (continued)

8.3.13 Over-voltage Protection

If the output voltage at the V_{OUT} pin is detected above over-voltage protection threshold, typically 21 V, the TPS61178x stops switching immediately until the voltage at the V_{OUT} pin drops lower than the output over-voltage protection threshold (with 500mV hysteresis). This function prevents the devices against the over-voltage and secures the circuits connected to the output from excessive over voltage.

8.3.14 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 150°C. When the thermal shutdown is triggered, the device stops switching and recover when the junction temperature falls below 130°C (typical).

8.4 Device Functional Modes

8.4.1 Operation

TPS61178x operates at the peak current-mode pulse-width-modulation (PWM). At the beginning of each switching cycle, the low-side FET switch turns on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. The PWM controller turns off the low-side FET when the peak inductor current reaches a threshold level set by the error amplifier output. After the low-side FET turns off, the high-side synchronous FET is turned on after a short dead time until the beginning of the next oscillator clock cycle or until the inductor current reaches the reverse current sense threshold.

During the portion of the switching cycle when the low-side FET is on, the input voltage is applied across the inductor and stores the energy as the inductor current ramps up. Meanwhile only the output capacitor supplies the load current. When it turns off the low-side FET, the inductor transfers the stored energy via the high-side synchronous FET to replenish the output capacitor and also supply the load current. This operation repeats every switching cycle.

The device features the internal slope compensation to avoid sub-harmonic oscillation that is intrinsic to peak-current mode control at duty cycle larger than 50%. The internal slope compensation may not be adequate to maintain stability for a very low inductance in application.

At the light load condition, the TPS61178x implements two options: Auto PFM mode (TPS61178) and Forced PWM mode (TPS611781) to meet different application requirements.

8.4.2 Auto PFM Mode (TPS61178)

The TPS61178 integrates a Power Save Mode with pulse frequency modulation (PFM) at the light load. When a light load condition occurs, the COMP pin voltage naturally decreases and reduces the peak current. When the COMP pin voltage further goes down with the load lowered and reaches the pre-set low threshold, the output of the error amplifier is clamped at this threshold and does not go down any more. If the load is further lowered, the output voltage of TPS61178 exceeds the nominal voltage and the device skips the switching cycles and regulate the output voltage at a higher threshold (typical 101%*V_{OUT_NORMAL}).

The Auto PFM mode reduces the switching losses and improves efficiency at the light load condition by reducing the average switching frequency.

8.4.3 Forced PWM Mode (TPS611781)

In the Forced PWM mode, the TPS611781 keeps the switching frequency being constant for the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power from input to output. The high-side FET is not turned off even if the current through the FET goes negative to keep the switching frequency being the same as that of the heavy load.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61178x family is the step up DC / DC converter. The following design procedure can be used to select component values for the TPS61178x. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an interactive design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

9.2 Typical Application

The application described is for 6-V to 14-V input, 16-V output converter.

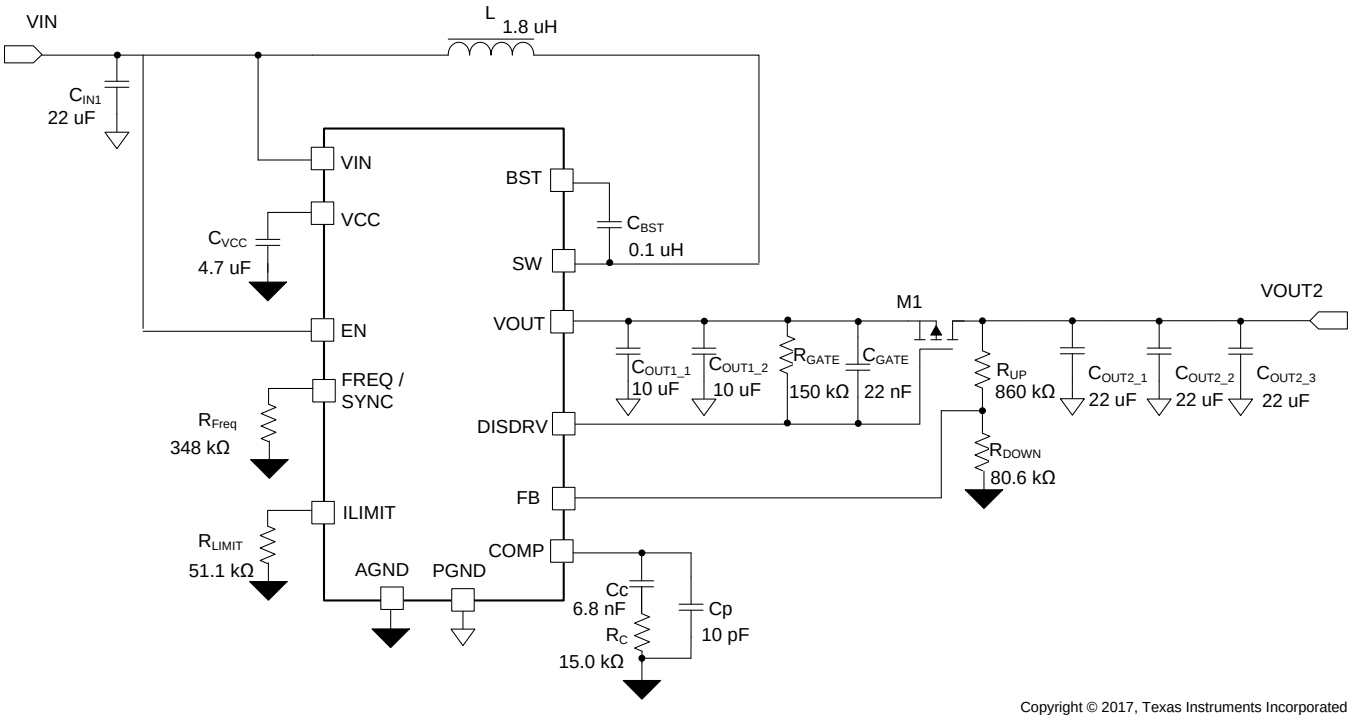

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Figure 22. TPS61178 16-V Output with Load Disconnect Schematic

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Typical Application (continued)

9.2.1 Design Requirements

For this design example, use Table 1 as the design parameters.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	6 V to 14 V
Output voltage	16 V
Output ripple voltage	±3%
Output current rating	3 A
Operating frequency	500 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61178 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Output ripple voltage
- Output current rating
- Operating frequency
- Load disconnect needed or not

9.2.2.2 Setting the Switching Frequency

The switching frequency of the TPS61178 is set at 500 kHz. Use Equation 2 to calculate the required resistor value. The calculated value is 342 kΩ. Use the next higher standard value of 348 kΩ.

9.2.3 Setting the Current Limit

The current limit of the TPS61178 could be programmed by an external resistor. For a target current limit of 13 A, the calculated resistor value is 57 kΩ. However, the minimum current limit is around 1.6 A lower than the typical one. Here, selecting the 51.1 kΩ resistor to deliver 13-A peak current at the worst case.

9.2.4 Setting the Output Voltage

The output voltage of the TPS61178 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by Equation 4.

$$V_{OUT} = V_{FB} \times (1 + \frac{R_{UP}}{R_{DOWN}})$$

where

- V_{OUT} is the output voltage
- R_{UP} the top divider resistor
- R_{DOWN} is the bottom divider resistor (4)

Choose R_{DOWN} to be approximately 80.6 kΩ. Slightly increasing or decreasing R_{DOWN} can result in closer output voltage matching when using standard value resistors. In this design, R_{DOWN} = 80.6 kΩ and R_{UP} = 1000 kΩ, resulting in an output voltage of 16 V.

For the best accuracy, R_{DOWN} is recommended to be smaller than 100 kΩ to ensure that the current following through R_{DOWN} is at least 100 times larger than FB pin leakage current. Changing R_{DOWN} towards the lower value increases the robustness against noise injection. Changing the R_{DOWN} towards the higher values reduces the quiescent current for achieving higher efficiency at the light load currents.

9.2.4.1 Selecting the Inductor

A boost converter normally requires two main passive components for storing the energy during the power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency) as well as the transient behavior and loop stability, which makes the inductor to be the most critical component in application.

When selecting the inductor, as well as the inductance, the other parameters of importance are:

- The maximum current rating (RMS and peak current should be considered),
- The series resistance,
- Operating temperature

Choosing the inductor ripple current with the low ripple percentage of the average inductor current results in a larger inductance value, maximizes the converter's potential output current and minimizes EMI. The larger ripple results in a smaller inductance value, and a physically smaller inductor, improves transient response but results in potentially higher EMI.

The rule of thumb to choose the inductor is that to make the inductor ripple current (ΔIL) is a certain percentage (Ripple % = 20 – 30 %) of the average current. The inductance can be calculated by Equation 5, Equation 6, and Equation 7:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{5}$$

$$\Delta I_{L_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{6}$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}}$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple % is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency (7)

The current flowing through the inductor is the inductor ripple current plus the average input current. During power-up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

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The TPS61178x has built-in slope compensation to avoid sub-harmonic oscillation associated with the current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 4 A, the slope compensation may not be adequate, and the loop can be unstable. Therefore, it is recommended to make the peak-to-peak current ripple below 4 A when selecting the inductor.

Inductor values can have ± 20% or even ± 30% tolerance with no current bias. When the inductor current approaches the saturation level, its inductance can decrease 20% to 35% from the value at 0-A bias current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, the switching frequency, the input and output voltages and it can be calculated by Equation 8 and Equation 9.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- Δ_{IL} is the ripple current of the inductor (8)

The input DC current is determined by the output voltage, the output current and efficiency can be calculated by :

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency (9)

While the inductor ripple current depends on the inductance, the frequency, the input voltage and duty cycle calculated by Equation 5, replace Equation 5, Equation 9 into Equation 8 and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor
- f_{SW} is the switching frequency (10)

The heat rating current (RMS) is as below:

$$I_{L_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2}$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- Δ_{IL} is the ripple current of the inductor (11)

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print.

The following inductor series in Table 2 from the different suppliers are recommended. 74437368033 from Würth is used for this application case with balancing the size and power loss.

Table 2. Recommended Inductors for TPS61178x(1)

PART NUMBER	L (µH)	DCR Typ (mΩ) Max	SATURATION CURRENT / Heat Rating Current (A)	SIZE (L × W × H mm)	VENDOR(1)
744325180	1.8	3.5	18	5 x 10 x 4	Würth
74437368033	3.3	11.8	23 / 8	10 x 10 x 3.8	Würth
DFEH10040D-3R3M#	3.3	12	10 / 10	10.9 x 10 x 4	Murata / TOKO
PIMB104T-4R7MS	4.7	20.0	15 / 8.5	10.9 x 10 x 3.8	Cyntec
74437368068	6.8	17.5	14	11 x 10 x 3.8	Würth
74437368100	10	27	12.5	11 x 10 x 3.8	Würth

(1) See *Third-party Products Disclaimer*

9.2.4.2 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. Then the loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 12:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}}$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency (12)

The additional output ripple component caused by ESR is calculated by Equation 13:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR}$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor (13)

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using Equation 14:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}}$$

where

- ΔI_{STEP} is the transient load current step

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- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (i.e., the frequency where the control loop gain crosses zero) (14)

Care must be taken when evaluating a ceramic capacitor's derating under the DC bias. Ceramic capacitors can derate by as much as 70% of its capacitance at its rated voltage. Therefore, enough margins on the voltage rating should be considered to ensure adequate capacitance at the required output voltage.

In applications of TPS61178x, it is recommended to run the converter with a reasonable amount of effective output capacitance, for instance 3 x 22-µF X5R or X7R MLCC capacitors connected in parallel.

If the load disconnect FET is connected, the output capacitor should be split shown in Figure 23. C_{OUT2} should be no larger than 10 x C_{OUT1} to avoid the inrush current when turning on the disconnect FET.

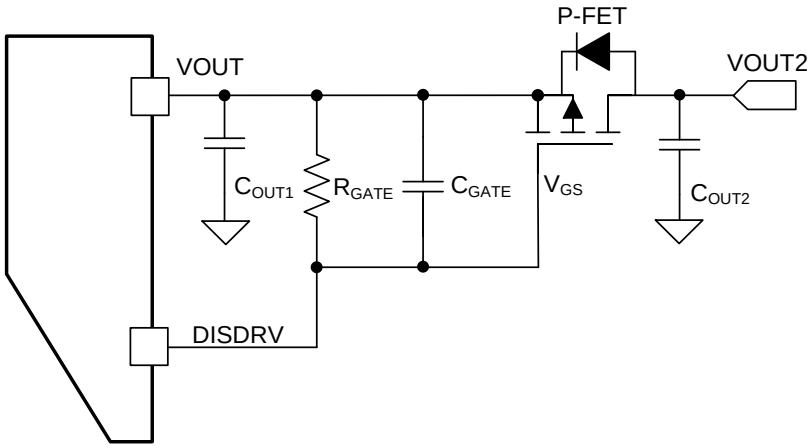

Figure 23. Output Capacitor Configuration with the Load Disconnect FET

9.2.4.3 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 22-µF input capacitor is sufficient for the most applications, larger values may be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, should be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

9.2.4.4 Loop Stability and Compensation

9.2.4.4.1 Small Signal Model

The TPS61178x uses the fixed frequency peak current mode control; there is an internal adaptive slope compensation to avoid the sub-harmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. Figure 24 shows the equivalent small signal elements of a boost converter.

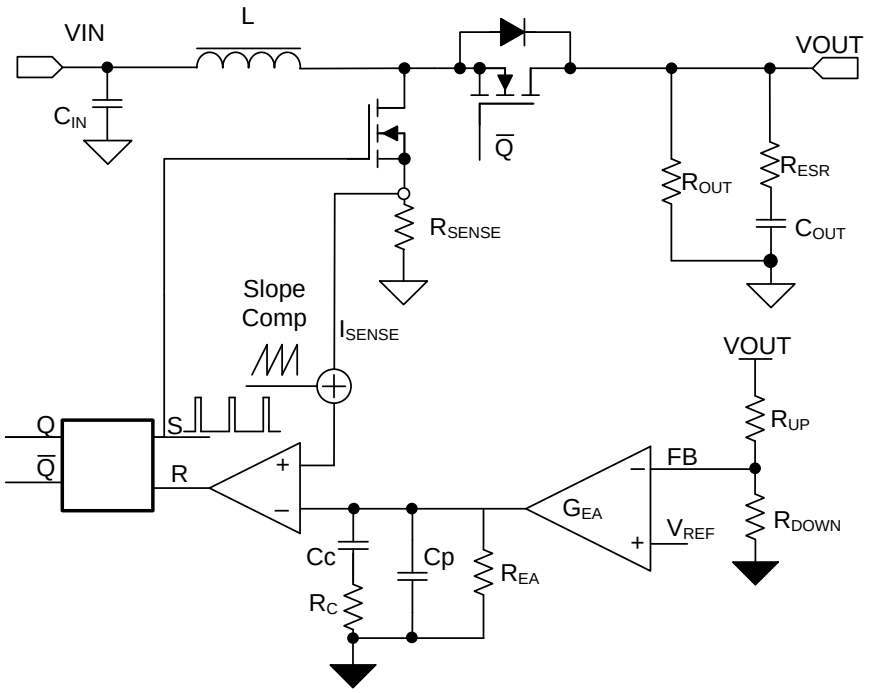

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Figure 24. TPS61178x Control Equivalent Circuitry Model

The small signal of power stage including the slope compensation is:

$$G_{PS}(S) = \frac{R_{OUT} \times (1 - D)}{2 \times R_{SENSE}} \times \frac{\left(1 + \frac{S}{2\pi \times f_{ESR}}\right)\left(1 - \frac{S}{2\pi \times f_{RHP}}\right)}{1 + \frac{S}{2\pi \times f_P}} \times He(S)$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- R_{SENSE} is the equivalent internal current sense resistor, which is typically 0.083 Ω of TPS61178x (15)

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}}$$

where

- C_{OUT} is the output capacitance, for a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance (16)

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor. (17)

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1 - D)^2}{2\pi \times L}$$

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where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance (18)

Using He(s) to model the inductor current sampling effect as well as the slope compensation effect on the small signal response, is shown in Equation 19

$$He(S) = \frac{1}{1 + \frac{S \times \left[(1 + \frac{Se}{Sn}) \times (1 - D) - 0.5 \right]}{f_{SW}} + \frac{S^2}{(\pi \times f_{SW})^2}} \tag{19}$$

$$Sn = \frac{V_{IN}}{L} \times R_{SENSE}$$

where

- Sn is the slew rate of the inductor current ramping up (20)

$$Se = 0.06 \times \frac{f_{SW}}{1 - D} \times R_{dson_LS}$$

where

- Se is the slope compensation slew rate
- R_{dson_LS} is the on resistance of Low-side FET (21)

The slope compensation adaptively changes with the switching frequency and duty cycle.

He(s) models the inductor current sampling effect as well as the slope compensation effect on the small signal response. Note that if Sn > Se, e.g., when L is too small, the converter operates as a voltage mode converter and the above model no longer holds.

The TPS61178x COMP pin is the output of the internal trans-conductance amplifier.

Equation 22 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2 \times \pi \times f_Z}}{(1 + \frac{S}{2 \times \pi \times f_{P1}}) \times (1 + \frac{S}{2 \times \pi \times f_{P2}})}$$

where

- k_{COMP} and R_{EA} are the ratio of peak current / comp voltage, for TPS61178x, the typical value is k_{COMP} = 12 A / V and R_{EA} = 20 MΩ.
- f_{P1}, f_{P2} is the pole's frequency of the compensation, f_Z is the zero's frequency of the compensation network. network (22)

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c}$$

where

- C_C is the zero capacitor compensation (23)

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P}$$

where

- C_P is the pole capacitor compensation
- R_C is the resistor of the compensation network (24)

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{25}$$

9.2.4.4.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Cross Over Frequency, f_C**
   - The first step is to set the loop crossover frequency, f_C. The higher crossover frequency, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. Then calculate the loop compensation network values of R_C, C_C, and C_P by following below equations.
2. **Set the Compensation Resistor, R_C**
   - By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} ~= R_C and so $R_C \times G_{EA}$ sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_Z, results in the total loop gain, $T_{(s)} = G_{PS(s)} \times H_{EA(s)} \times He(s)$ being zero at f_C.
   - Therefore, to approximate a single-pole roll-off up to f_{P2}, rearrange Equation 22 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}, read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \tag{26}$$

   where
   - K_{EA} is gain of the error amplifier network
   - K_{PS} is the gain of the power stage
   - G_{EA} is the amplifier's trans-conductance, the typical value of G_{EA} = 195 µA / V
3. **Set the compensation zero capacitor, C_C**
   - Place the compensation zero at the power stage R_{OUT} ,C_{OUT} pole's position, so to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{27}$$

   - Set $f_Z = f_P$, and get the

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \tag{28}$$

4. **Set the compensation pole capacitor, C_P**
   - Place the compensation pole at the zero produced by the R_{ESR} and the C_{OUT}, it is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \tag{29}$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{30}$$

   - Set $f_{P2} = f_{ESR}$, and get the

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \tag{31}$$

   - If the calculated value of C_P is less than 10 pF, it can be neglected.

   Designing the loop for greater than 45° of phase margin and greater than 6-dB gain margin eliminates output voltage ringing during the line and load transient. The R_C = 15 kΩ , C_C = 6.8 nF, C_p = 10 pF for this design example.

9.2.4.4.3 Selecting the Disconnect FET

The TPS61178x provides a gate driver to control an external FET to disconnect the output from the input at shutdown or output short conditions, shown in Figure 25.

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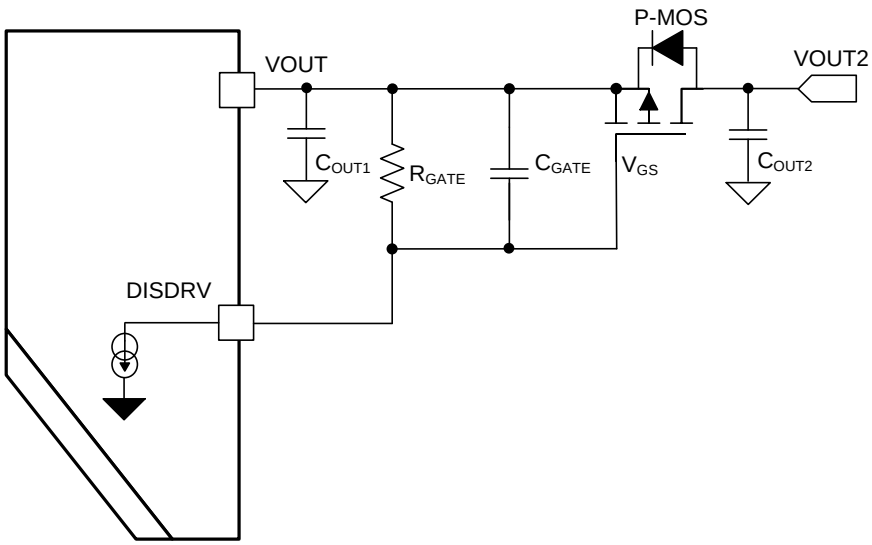


Figure 25. Load Disconnect FET Connection

The V_{DS}, I_{DS} and safe operation area (SOA) should be taken into consideration when selecting the FET:

- The drain-to-source voltage rating should be higher than the output max. voltage, $V_{DS_DIS_MAX} = V_{OUT}$,
- The drain-to-source RMS current rating is the maximum output current. $I_{DS_DIS_RMS} = I_{OUT}$,
- The SOA should be considered when the output short occurs, and there is heat caused by the short protection response time and surge current, SOA > Q_{SHORT}.

$$Q_{SHORT} = \frac{1}{2} \times V_{OUT} \times I_{SHORT} \times T_{SHORT}$$

where

- $V_{DS_DIS_Max}$ is the maximum drain-source voltage
- I_{DS_DIS} is the drain-source RMS current
- I_{SHORT} is the short current
- T_{SHORT} is the response time before the short protection triggered
- Q_{SHORT} is the heat produced for the output short (32)

For instance: V_{OUT} = 16 V, I_{SHORT} = 20 A , T_{SHORT} = 30 µs.
SOA ≥ 4.8 mJ, $V_{DS_DIS_MAX}$ ≥ 16 V.
The CSD25404Q3 –20 V P-Channel NexFET™ Power FET is used for this design example.

An additional capacitor between the gate and source of the external FET is required to slow the turn-on speed.

$$T_{ON_PFET} = \frac{V_{TH_PFET} \times C_{GS_PFET}}{I_{DIS_PFET}}$$

where

- T_{ON_PFET} is the on time of external FET
- V_{TH_PFET} is the gate threshold of external FET
- C_{GS_PFET} is the total gate capacitance of connected between gate and source external FET. (including the self-gate-source capacitance of the FET)
- $_{IDIS_PFET}$ is the discharge current inside of TPS61178x, it is 55 µA typically (33)

Given 1.5 V threshold, C_{GS_PFET} is 10 nF, the T_{ON_PFET} is around 300 µs.Please be aware that the maximum turn-on time should not exceed 3 ms, and the maximum capacitance C_{GS_PFET} should be < 100 nF. Otherwise, the TPS61178x could not startup normally if the disconnect FET could not be turn on within the 3 ms.

The gate resistor depends on the gate-source voltage of the external FET,

$$V_{GATE} = R_{GATE} \times I_{DIS_PFET} \quad (34)$$

$$R_{GATE} = \frac{V_{GATE}}{I_{DIS_PFET}} \tag{35}$$

Given the 5-V V_{GATE}, the R_{GATE} = 100 kΩ

9.2.4.4.4 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during each cycle's turn-on and also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1 µF to 1 µF. C_{BST} should be a good quality, low ESR, ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1 µF was selected for this design example.

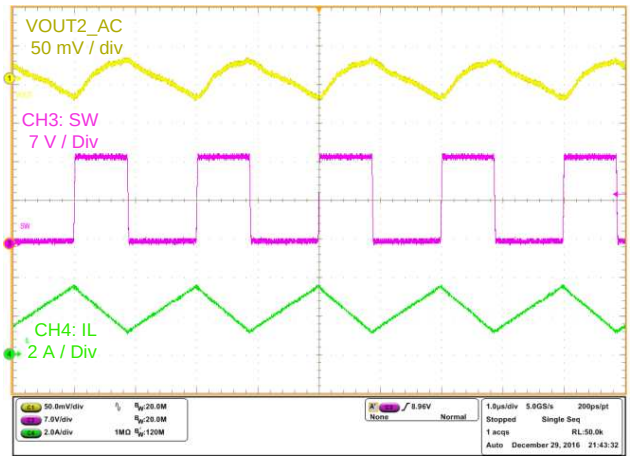
9.2.4.4.5 V_{CC} Capacitor

The primary purpose of the V_{CC} capacitor is to supply the peak transient currents of the driver and bootstrap capacitor as well as provide stability for the V_{CC} regulator. The value of C_{VCC} should be at least 10 times greater than the value of C_{BST}, and should be a good quality, low ESR, ceramic capacitor. C_{VCC} should be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 4.7 µF was selected for this design example.

9.2.5 TPS61178 Application Waveform

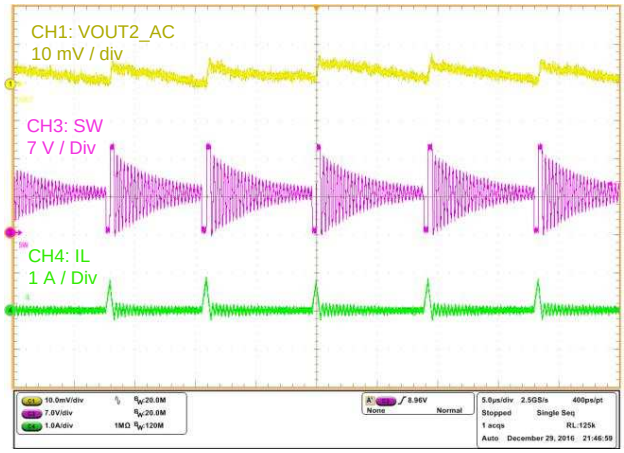
Typical condition V_{IN} = 6 V to 14 V, V_{OUT} = 16 V, R_{LIMIT} = 51.1 kΩ, R_{FREQ} = 348 kΩ

Application waveforms are measured with the inductor 3.3 µH, Würth 74437368033, and the output capacitance: 3 x 22 µF, GRM32ER61E226KE15L plus 2 x 10 µF, GRM188R61E106MA73D.



V_{IN} = 7.2 V V_{OUT}= 16 V
L = 3.3 µH C_{OUT}= 86 µF Load = 1000 mA

Figure 26. Steady State 1000 mA



V_{IN} = 7.2 V V_{OUT}= 16 V Auto PFM
L = 3.3 µH C_{OUT}= 86 µF Load = 10 mA

Figure 27. Steady-state 10 mA

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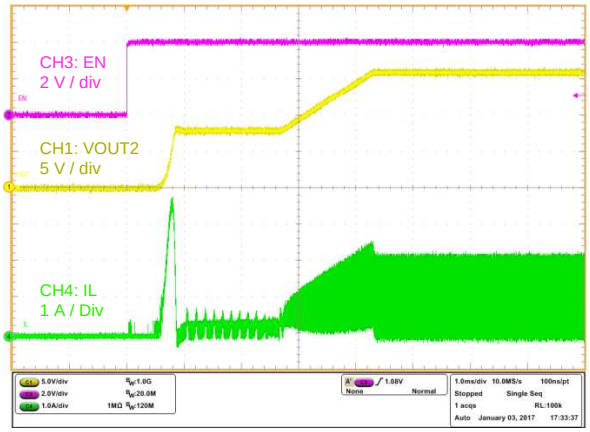
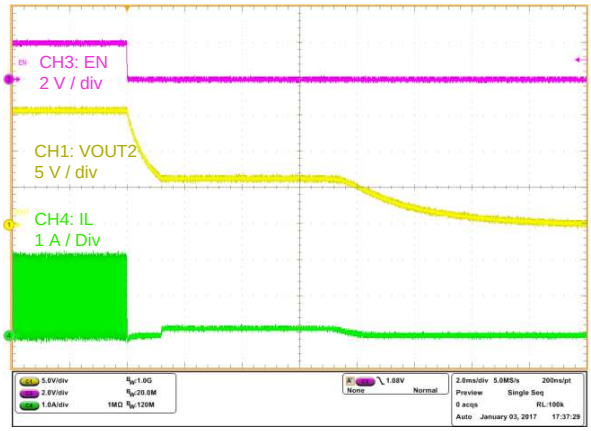


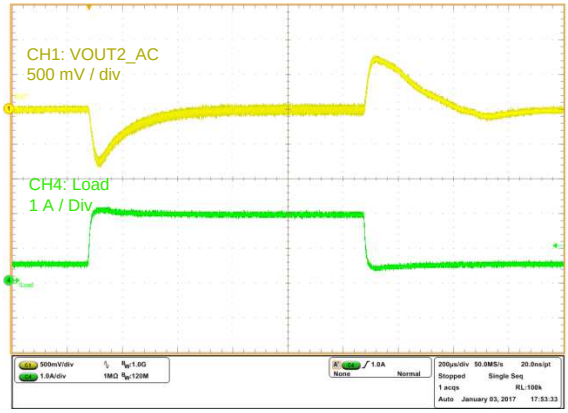
V_{IN} = 7.2 V V_{OUT}= 16 V Auto PFM
L = 3.3 µH C_{OUT}= 86 µF Load = 32 Ω

Figure 28. Startup by EN



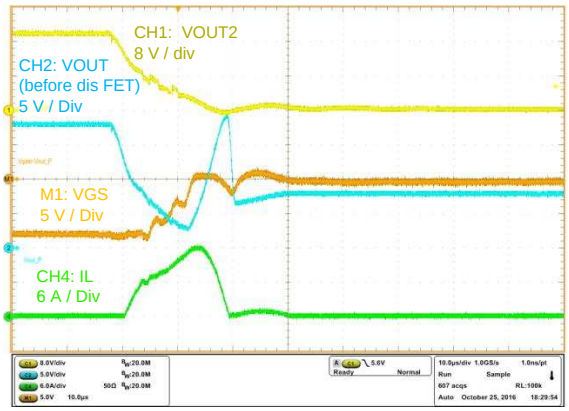
V_{IN} = 7.2 V V_{OUT}= 16 V Auto PFM
L = 3.3 µH C_{OUT}= 86 µF Load = 32 Ω

Figure 29. Shutdown by EN



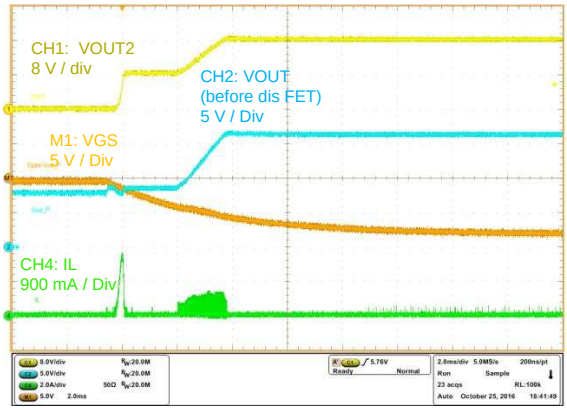
V_{IN} = 7.2 V V_{OUT}= 16 V Load = 500 mA to 2 A,
L = 3.3 µH C_{OUT}= 86 µF 0.1 A/µs slew rate

Figure 30. Load Transient



V_{IN} = 7.2 V V_{OUT}= 16 V
L = 3.3 µH C_{OUT}= 86 µF

Figure 31. Output Short (with Disconnect FET)



V_{IN} = 7.2 V V_{OUT}= 16 V
L = 3.3 µH C_{OUT}= 86 µF

Figure 32. Output Short Release (with Disconnect FET)

9.3 System Examples

9.3.1 TPS61178 with 14-V Output from 2.7-V to 4.4-V Input Voltage

The Figure 33 is the typical application schematic for 2.7-V to 4.4-V input (single cell Li+ battery) to output 14-V output converter. The inductor can be lower to 1.8 µH for the 14-V output.

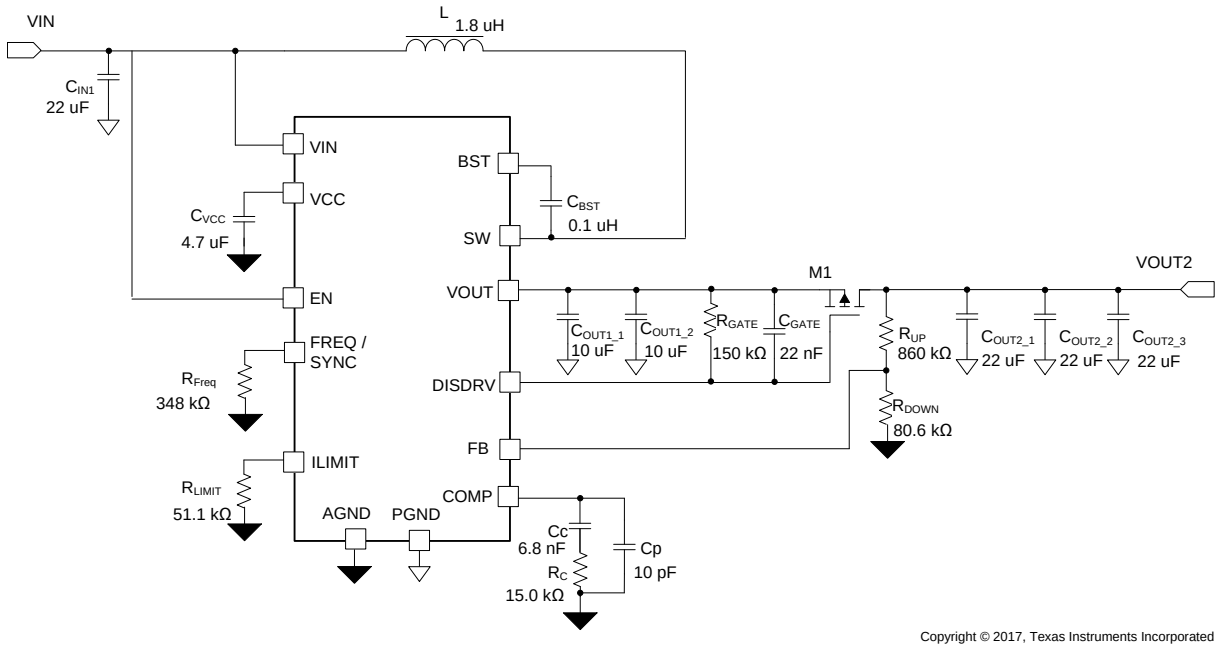


Figure 33. 14-V Output Voltage from 2.7-V to 4.4-V Input Voltage

9.3.2 TPS61178 Without Load Disconnect Function

The Figure 34 is the typical application schematic is for 6-V to 14-V input (2 / 3 cells Li+ battery or 12-V bus) to output 14-V output converter without load disconnect. With removing the load disconnect FET, it simplifies the design and minimizes the external components.

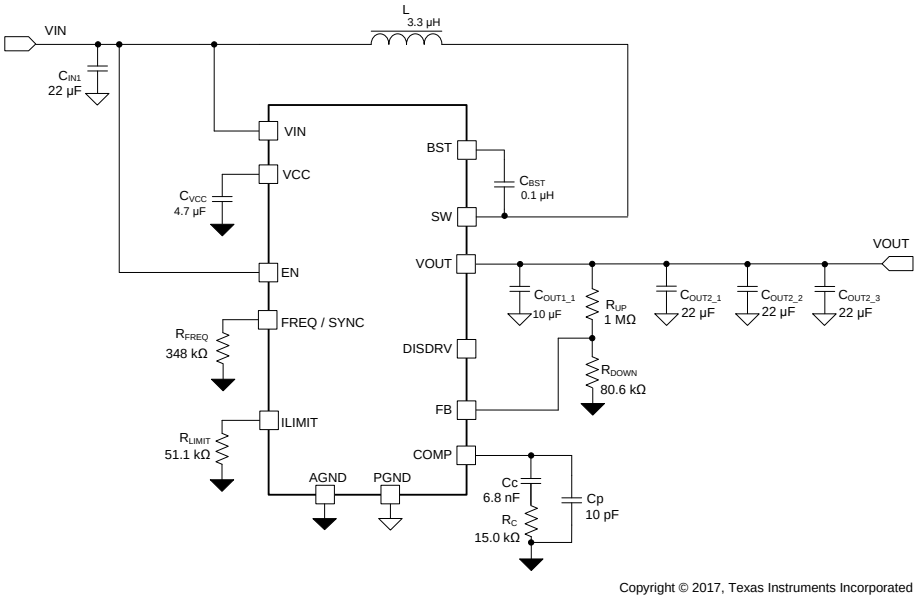


Figure 34. 16-V Output Voltage Without Load Disconnect Function

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System Examples (continued)

9.3.3 TPS611781 External Clock Synchronization

The Figure 35 is the typical application schematic for synchronized by an external clock of 2.2 MHz. It is for the Forced PWM mode operation to avoid the noise-sensitive frequency range, for instance the audible noise and AM band.

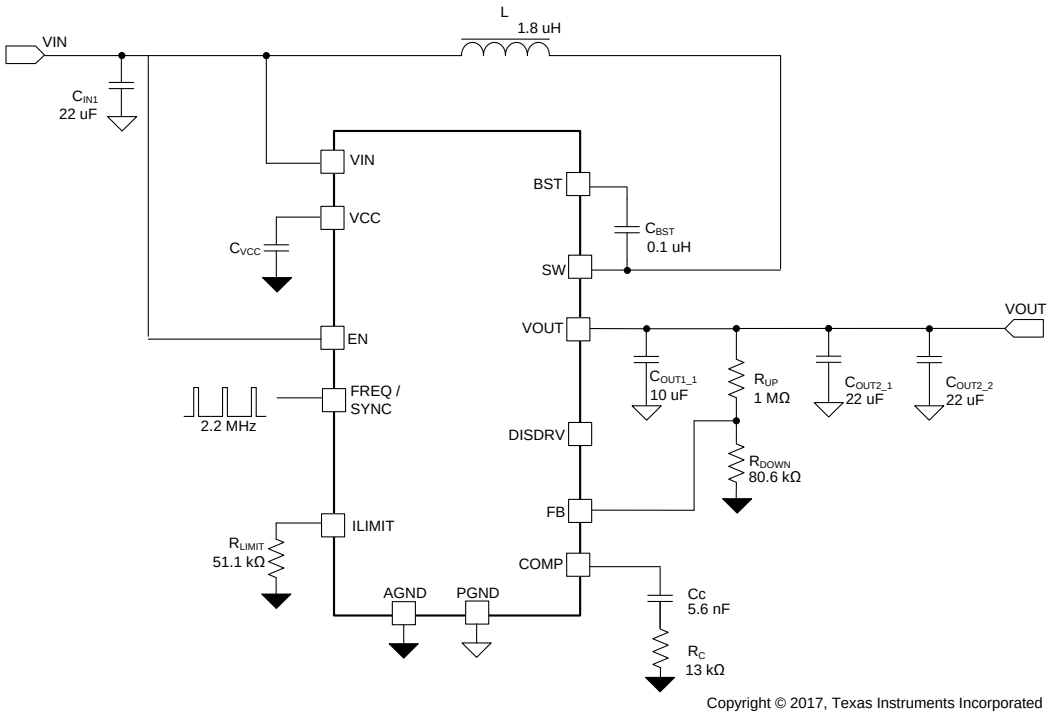

Figure 35. 16-V Output Voltage Synchronized by 2.2 MHz External Clock

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply ranging from 2.7 V to 20 V. This input supply should be well regulated. If the input supply is located more than a few inches from the TPS61178x, the bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems.

The checklist below is suggested that be followed to get good performance for a well-designed board:

1. Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di/dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;
2. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize inter plane coupling;
3. Use a combination of bulk capacitors and smaller ceramic capacitors with low series resistance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for decoupling the noise;
4. The ground area near the IC must provide adequate heat dissipating area. Connect the wide power bus (e.g., V_{OUT}, SW, GND) to the large area of copper, or to the bottom or internal layer ground plane, using vias for enhanced thermal dissipation;
5. Place the input capacitor being close to the V_{IN} pin and the PGND pin in order to reduce the input supply ripple;
6. Place the noise sensitive network like the feedback and compensation being far away from the SW trace;
7. Use a separate ground trace to connect the feedback, compensation, frequency set, and the current limit set circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

11.2 Layout Example

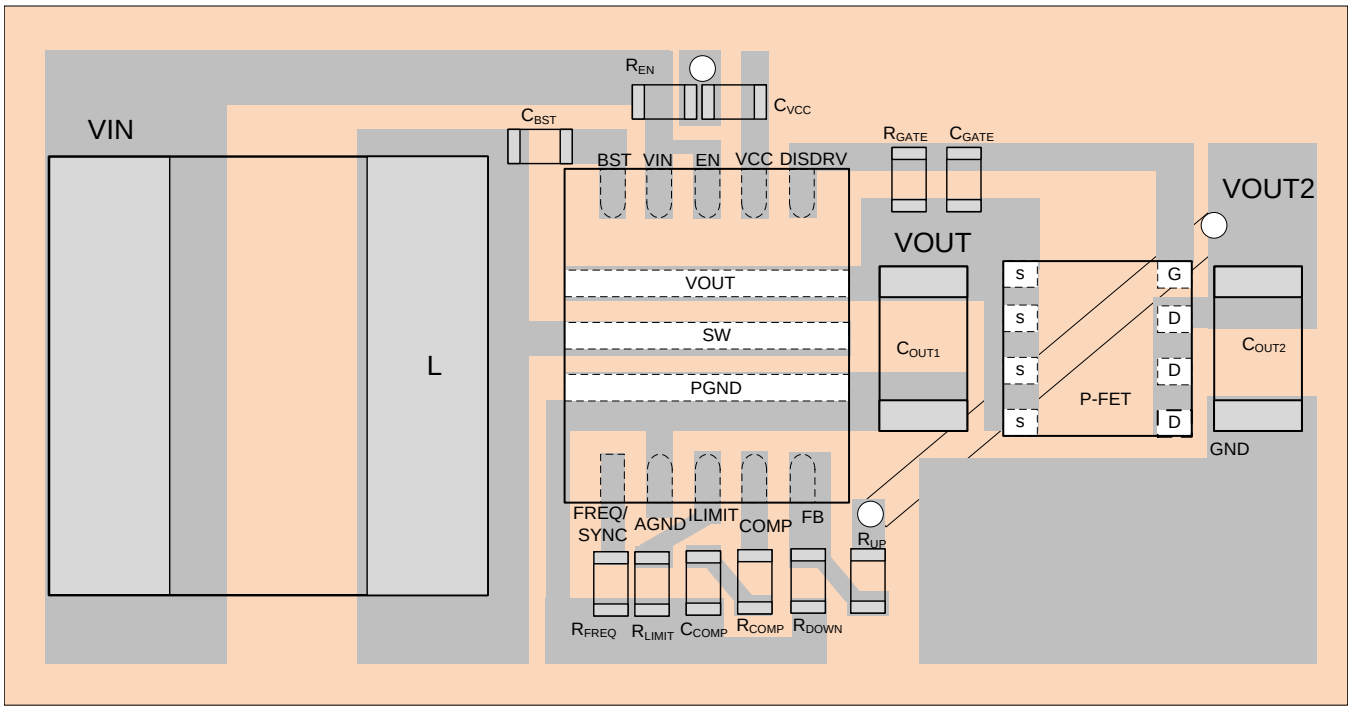

Figure 36. Recommended Layout

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61178 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- TPS61178EVM Evaluation Board User's Guide, SLVUB05
-

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 3. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61178	Click here	Click here	Click here	Click here	Click here
TPS611781	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS611781RNWR	Active	Production	VQFN-HR (RNW) | 13	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	1CDI
TPS611781RNWR.A	Active	Production	VQFN-HR (RNW) | 13	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1CDI
TPS611781RNWT	Active	Production	VQFN-HR (RNW) | 13	250 | SMALL T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	1CDI
TPS611781RNWT.A	Active	Production	VQFN-HR (RNW) | 13	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1CDI
TPS61178RNWR	Active	Production	VQFN-HR (RNW) | 13	3000 | LARGE T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	15RI
TPS61178RNWR.A	Active	Production	VQFN-HR (RNW) | 13	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	15RI
TPS61178RNWT	Active	Production	VQFN-HR (RNW) | 13	250 | SMALL T&R	Yes	Call TI | Sn	Level-2-260C-1 YEAR	-40 to 125	15RI
TPS61178RNWT.A	Active	Production	VQFN-HR (RNW) | 13	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	15RI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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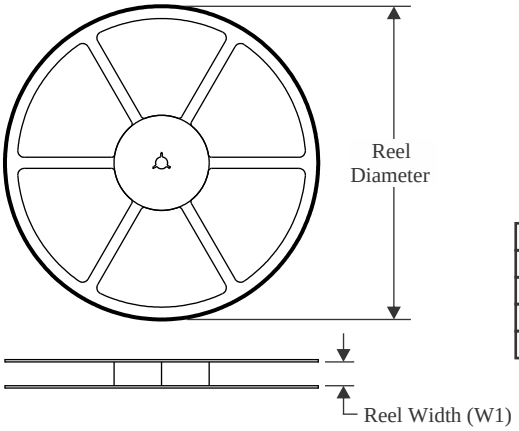
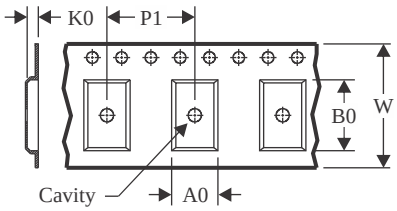
TAPE AND REEL INFORMATION

REEL DIMENSIONS

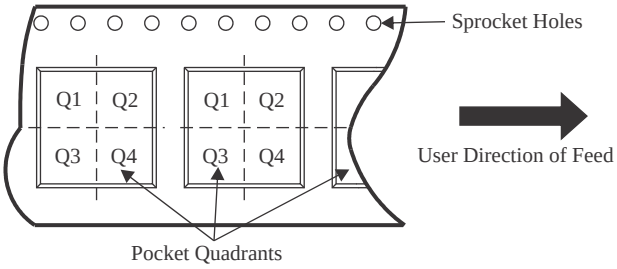


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

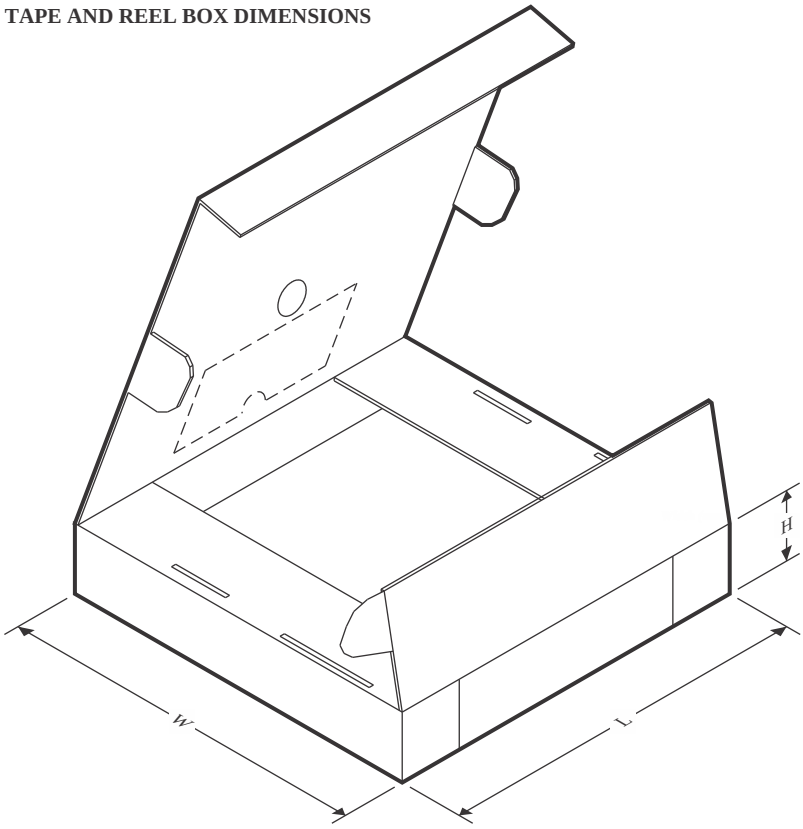
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

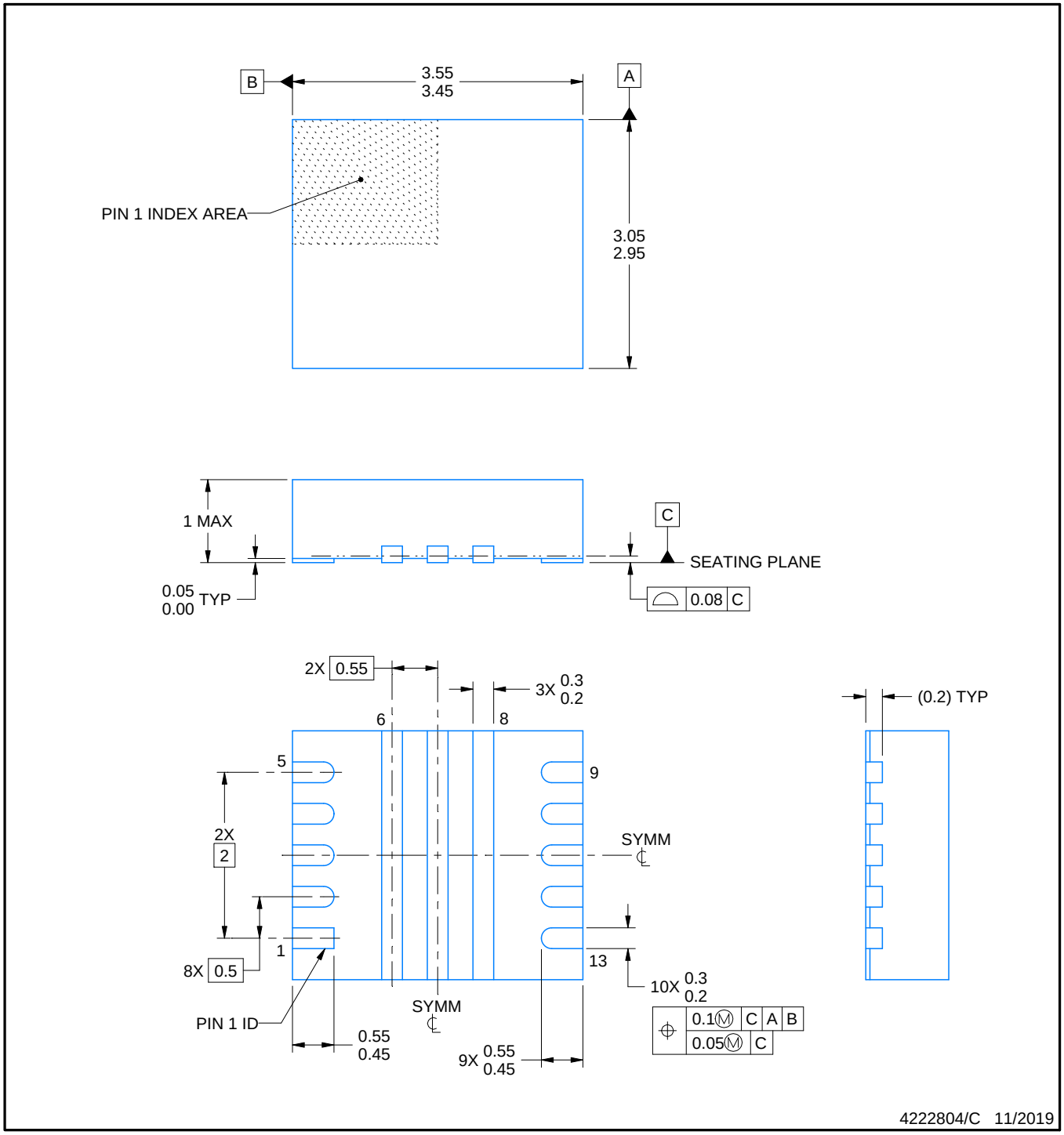
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS611781RNWT	VQFN-HR	RNW	13	250	180.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2
TPS61178RNWR	VQFN-HR	RNW	13	3000	330.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2
TPS61178RNWT	VQFN-HR	RNW	13	250	180.0	12.4	3.3	3.8	1.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



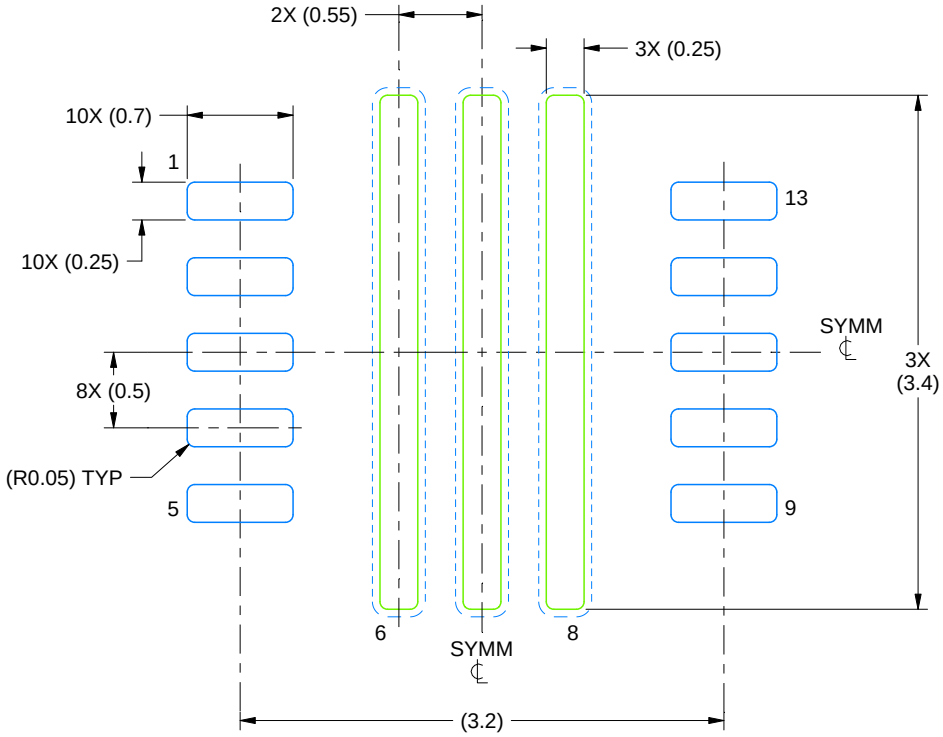
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS611781RNWT	VQFN-HR	RNW	13	250	341.0	185.0	80.0
TPS61178RNWR	VQFN-HR	RNW	13	3000	346.0	346.0	80.0
TPS61178RNWT	VQFN-HR	RNW	13	250	341.0	185.0	80.0

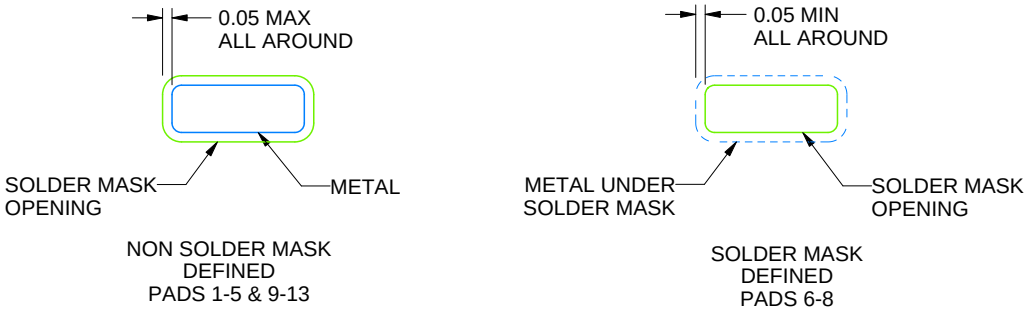


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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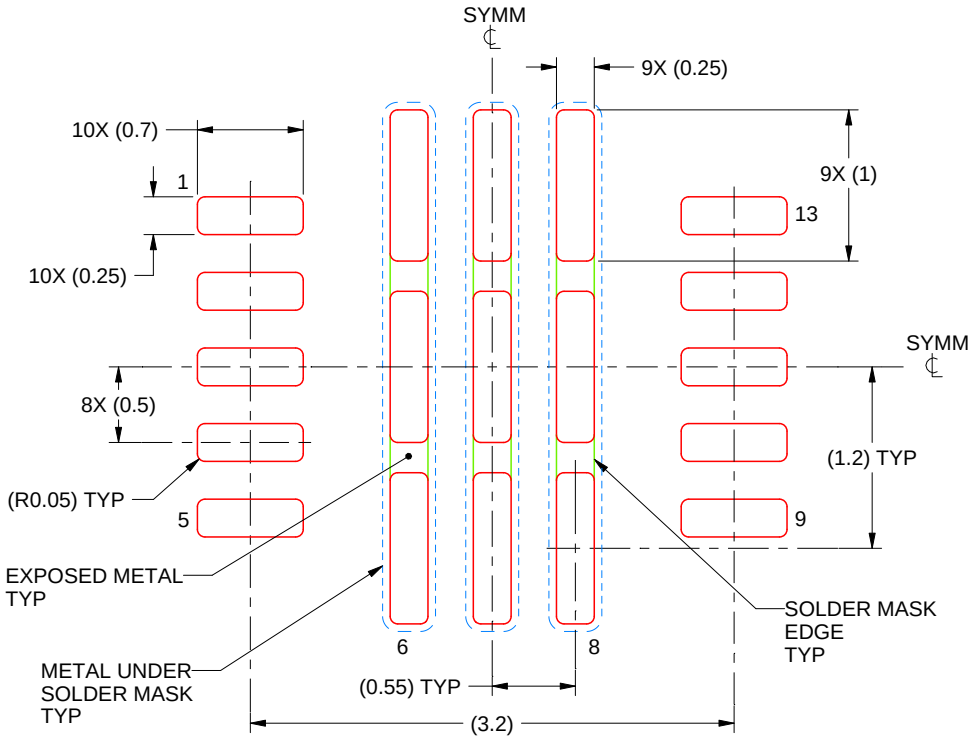
NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PADS 6-8
87% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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