

# SN54AHC595, SN74AHC595 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS373I – MAY 1997 – REVISED JUNE 2004

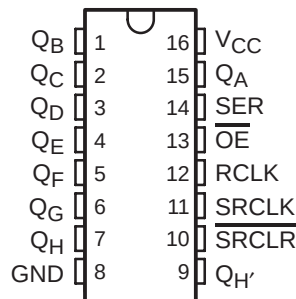
- Operating Range 2-V to 5.5-V  $V_{CC}$
- 8-Bit Serial-In, Parallel-Out Shift
- Shift Register Has Direct Clear
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## description/ordering information

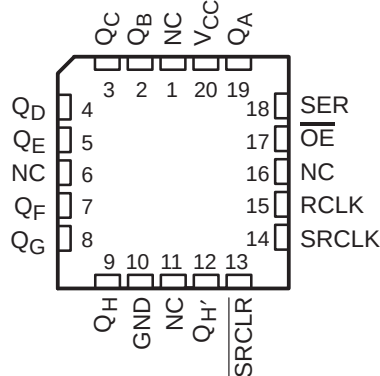
The 'AHC595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and a serial output for cascading. When the output-enable ( $\overline{OE}$ ) input is high, all outputs, except  $Q_{H'}$ , are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

SN54AHC595 . . . J OR W PACKAGE  
SN74AHC595 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AHC595 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†   |               | ORDERABLE<br>PART NUMBER | TOP-SIDE<br>MARKING |
|----------------|------------|---------------|--------------------------|---------------------|
| –40°C to 85°C  | PDIP – N   | Tube          | SN74AHC595N              | SN74AHC595N         |
|                | SOIC – D   | Tube          | SN74AHC595D              | AHC595              |
|                |            | Tape and reel | SN74AHC595DR             |                     |
|                | SOP – NS   | Tape and reel | SN74AHC595NSR            | AHC595              |
|                | SSOP – DB  | Tape and reel | SN74AHC595DBR            | HA595               |
|                | TSSOP – PW | Tube          | SN74AHC595PW             | HA595               |
| Tape and reel  |            | SN74AHC595PWR |                          |                     |
| –55°C to 125°C | CDIP – J   | Tube          | SNJ54AHC595J             | SNJ54AHC595J        |
|                | CFP – W    | Tube          | SNJ54AHC595W             | SNJ54AHC595W        |
|                | LCCC – FK  | Tube          | SNJ54AHC595FK            | SNJ54AHC595FK       |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
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# SN54AHC595, SN74AHC595

## 8-BIT SHIFT REGISTERS

### WITH 3-STATE OUTPUT REGISTERS

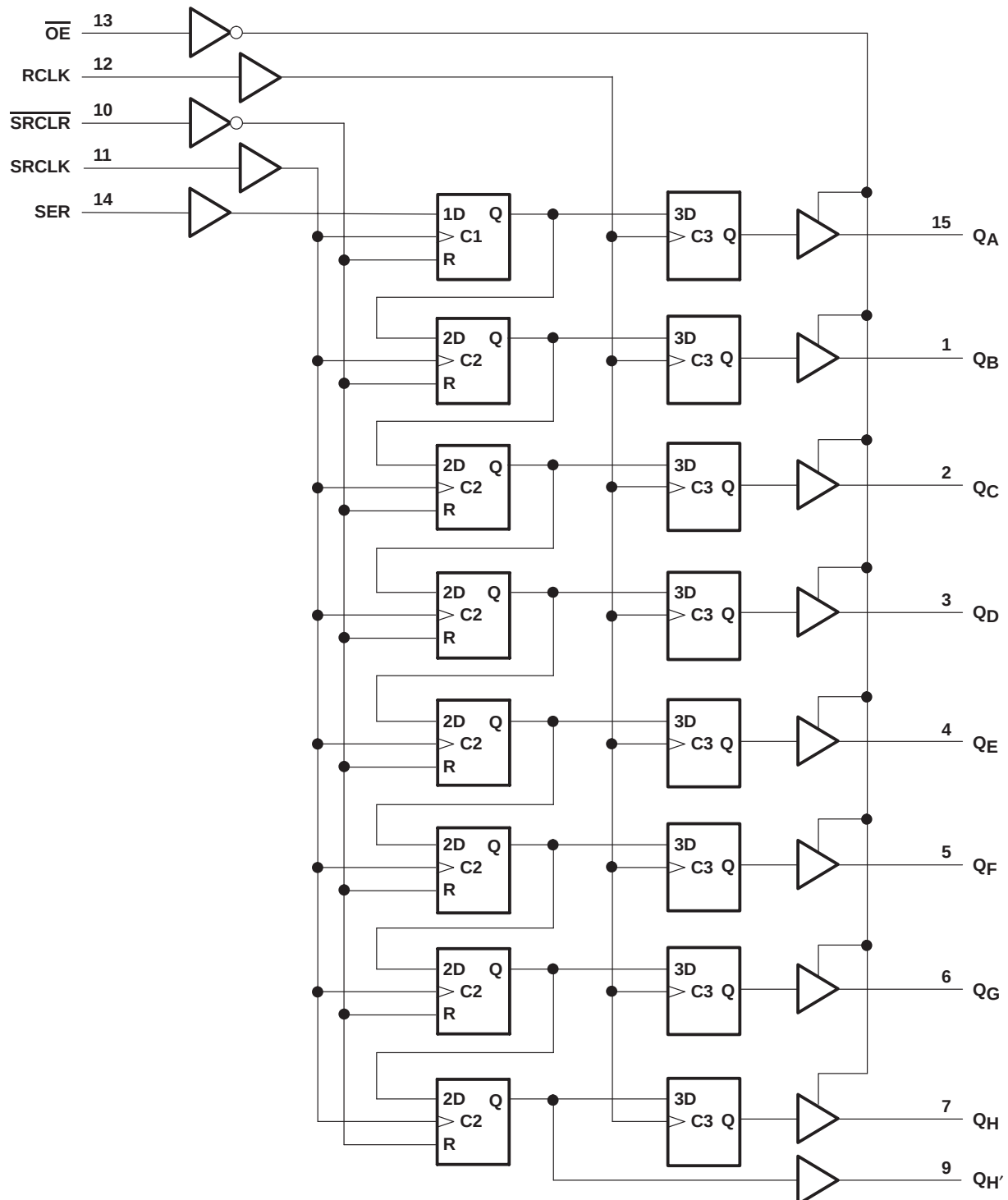
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FUNCTION TABLE

| INPUTS |       |                           |      |                        | FUNCTION                                                                                                     |
|--------|-------|---------------------------|------|------------------------|--------------------------------------------------------------------------------------------------------------|
| SER    | SRCLK | $\overline{\text{SRCLR}}$ | RCLK | $\overline{\text{OE}}$ |                                                                                                              |
| X      | X     | X                         | X    | H                      | Outputs $Q_A$ – $Q_H$ are disabled.                                                                          |
| X      | X     | X                         | X    | L                      | Outputs $Q_A$ – $Q_H$ are enabled.                                                                           |
| X      | X     | L                         | X    | X                      | Shift register is cleared.                                                                                   |
| L      | ↑     | H                         | X    | X                      | First stage of the shift register goes low.<br>Other stages store the data of previous stage, respectively.  |
| H      | ↑     | H                         | X    | X                      | First stage of the shift register goes high.<br>Other stages store the data of previous stage, respectively. |
| X      | X     | X                         | ↑    | X                      | Shift-register data is stored into the storage register.                                                     |

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**logic diagram (positive logic)**



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

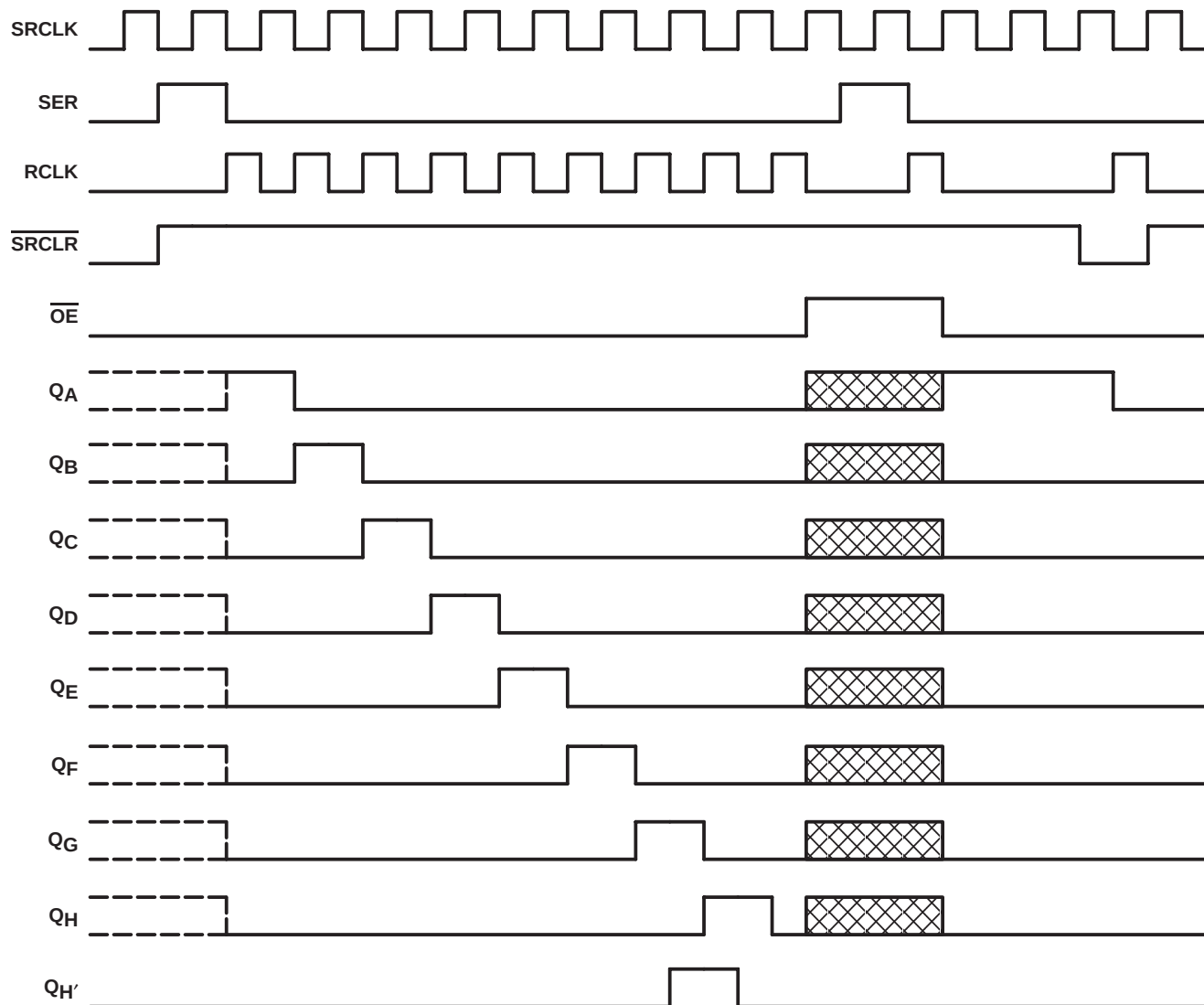
# SN54AHC595, SN74AHC595

## 8-BIT SHIFT REGISTERS

### WITH 3-STATE OUTPUT REGISTERS

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#### timing diagram



NOTE:  implies that the output is in 3-State mode.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

|                                                                  |                            |
|------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$                                   | –0.5 V to 7 V              |
| Input voltage range, $V_I$ (see Note 1)                          | –0.5 V to 7 V              |
| Output voltage range, $V_O$ (see Note 1)                         | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                      | –20 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )   | ±20 mA                     |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )       | ±25 mA                     |
| Continuous current through $V_{CC}$ or GND                       | ±75 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package | 73°C/W                     |
| DB package                                                       | 82°C/W                     |
| N package                                                        | 67°C/W                     |
| NS package                                                       | 64°C/W                     |
| PW package                                                       | 108°C/W                    |
| Storage temperature range, $T_{stg}$                             | –65°C to 150°C             |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

|                     |                                    |                          | SN54AHC595 |          | SN74AHC595 |          | UNIT |
|---------------------|------------------------------------|--------------------------|------------|----------|------------|----------|------|
|                     |                                    |                          | MIN        | MAX      | MIN        | MAX      |      |
| $V_{CC}$            | Supply voltage                     |                          | 2          | 5.5      | 2          | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 2$ V           | 1.5        |          | 1.5        |          | V    |
|                     |                                    | $V_{CC} = 3$ V           | 2.1        |          | 2.1        |          |      |
|                     |                                    | $V_{CC} = 5.5$ V         | 3.85       |          | 3.85       |          |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 2$ V           |            | 0.5      |            | 0.5      | V    |
|                     |                                    | $V_{CC} = 3$ V           |            | 0.9      |            | 0.9      |      |
|                     |                                    | $V_{CC} = 5.5$ V         |            | 1.65     |            | 1.65     |      |
| $V_I$               | Input voltage                      |                          | 0          | 5.5      | 0          | 5.5      | V    |
| $V_O$               | Output voltage                     |                          | 0          | $V_{CC}$ | 0          | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 2$ V           |            | –50      |            | –50      | µA   |
|                     |                                    | $V_{CC} = 3.3$ V ± 0.3 V |            | –4       |            | –4       | mA   |
|                     |                                    | $V_{CC} = 5$ V ± 0.5 V   |            | –8       |            | –8       |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 2$ V           |            | 50       |            | 50       | µA   |
|                     |                                    | $V_{CC} = 3.3$ V ± 0.3 V |            | 4        |            | 4        | mA   |
|                     |                                    | $V_{CC} = 5$ V ± 0.5 V   |            | 8        |            | 8        |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3$ V ± 0.3 V |            | 100      |            | 100      | ns/V |
|                     |                                    | $V_{CC} = 5$ V ± 0.5 V   |            | 20       |            | 20       |      |
| $T_A$               | Operating free-air temperature     |                          | –55        | 125      | –40        | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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## 8-BIT SHIFT REGISTERS

### WITH 3-STATE OUTPUT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                                                                                                                 | V <sub>CC</sub>                | T <sub>A</sub> = 25°C |     |       | SN54AHC595 |      | SN74AHC595 |      | UNIT |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------|--------------------------------|-----------------------|-----|-------|------------|------|------------|------|------|
|                 |                                                                                                                                 |                                | MIN                   | TYP | MAX   | MIN        | MAX  | MIN        | MAX  |      |
| V <sub>OH</sub> | I <sub>OH</sub> = -50 µA                                                                                                        | 2 V                            | 1.9                   | 2   |       | 1.9        |      | 1.9        |      | V    |
|                 |                                                                                                                                 | 3 V                            | 2.9                   | 3   |       | 2.9        |      | 2.9        |      |      |
|                 |                                                                                                                                 | 4.5 V                          | 4.4                   | 4.5 |       | 4.4        |      | 4.4        |      |      |
|                 | I <sub>OH</sub> = -4 mA                                                                                                         | 3 V                            | 2.58                  |     |       | 2.48       |      | 2.48       |      |      |
|                 | I <sub>OH</sub> = -8 mA                                                                                                         | 4.5 V                          | 3.94                  |     |       | 3.8        |      | 3.8        |      |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 50 µA                                                                                                         | 2 V                            |                       |     | 0.1   |            | 0.1  |            | 0.1  | V    |
|                 |                                                                                                                                 | 3 V                            |                       |     | 0.1   |            | 0.1  |            | 0.1  |      |
|                 |                                                                                                                                 | 4.5 V                          |                       |     | 0.1   |            | 0.1  |            | 0.1  |      |
|                 | I <sub>OL</sub> = 4 mA                                                                                                          | 3 V                            |                       |     | 0.36  |            | 0.5  |            | 0.44 |      |
|                 | I <sub>OL</sub> = 8 mA                                                                                                          | 4.5 V                          |                       |     | 0.36  |            | 0.5  |            | 0.44 |      |
| I <sub>I</sub>  | V <sub>I</sub> = 5.5 V or GND                                                                                                   | 0 V to 5.5 V                   |                       |     | ±0.1  |            | ±1*  |            | ±1   | µA   |
| I <sub>OZ</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND,<br>V <sub>O</sub> = V <sub>CC</sub> or GND,<br>OE = V <sub>IH</sub> or V <sub>IL</sub> | Q <sub>A</sub> -Q <sub>H</sub> | 5.5 V                 |     | ±0.25 |            | ±2.5 |            | ±2.5 | µA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                                                                     | 5.5 V                          |                       |     | 4     |            | 40   |            | 40   | µA   |
| C <sub>i</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                                         | 5 V                            |                       |     | 3     |            |      |            | 10   | pF   |
| C <sub>0</sub>  | V <sub>O</sub> = V <sub>CC</sub> or GND                                                                                         | 5 V                            |                       |     | 5.5   |            |      |            |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

timing requirements over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

|                 |                |                                     | T <sub>A</sub> = 25°C |     | SN54AHC595 |     | SN74AHC595 |     | UNIT |
|-----------------|----------------|-------------------------------------|-----------------------|-----|------------|-----|------------|-----|------|
|                 |                |                                     | MIN                   | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>w</sub>  | Pulse duration | SRCLK high or low                   | 5                     |     | 5          |     | 5          |     | ns   |
|                 |                | RCLK high or low                    | 5                     |     | 5          |     | 5          |     |      |
|                 |                | SRCLR low                           | 5                     |     | 5          |     | 5          |     |      |
| t <sub>su</sub> | Setup time     | SER before SRCLK↑                   | 3.5                   |     | 3.5        |     | 3.5        |     | ns   |
|                 |                | SRCLK↑ before RCLK↑†                | 8                     |     | 8.5        |     | 8.5        |     |      |
|                 |                | SRCLR low before RCLK↑              | 8                     |     | 9          |     | 9          |     |      |
|                 |                | SRCLR high (inactive) before SRCLK↑ | 3                     |     | 3          |     | 3          |     |      |
| t <sub>h</sub>  | Hold time      | SER after SRCLK↑                    | 1.5                   |     | 1.5        |     | 1.5        |     | ns   |

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

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**SN54AHC595, SN74AHC595**  
**8-BIT SHIFT REGISTERS**  
**WITH 3-STATE OUTPUT REGISTERS**  
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**timing requirements over recommended operating free-air temperature range,**  
 **$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

|                 |                | T <sub>A</sub> = 25°C               |     | SN54AHC595 |     | SN74AHC595 |     | UNIT |
|-----------------|----------------|-------------------------------------|-----|------------|-----|------------|-----|------|
|                 |                | MIN                                 | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>w</sub>  | Pulse duration | SRCLK high or low                   | 5   | 5          | 5   | 5          | 5   | ns   |
|                 |                | RCLK high or low                    | 5   | 5          | 5   | 5          | 5   |      |
|                 |                | SRCLR low                           | 5   | 5          | 5   | 5          | 5   |      |
| t <sub>su</sub> | Setup time     | SER before SRCLK↑                   | 3   | 3          | 3   | 3          | 3   | ns   |
|                 |                | SRCLK↑ before RCLK↑†                | 5   | 5          | 5   | 5          | 5   |      |
|                 |                | SRCLR low before RCLK↑              | 5   | 5          | 5   | 5          | 5   |      |
|                 |                | SRCLR high (inactive) before SRCLK↑ | 2.5 | 2.5        | 2.5 | 2.5        | 2.5 |      |
| t <sub>h</sub>  | Hold time      | SER after SRCLK↑                    | 2   | 2          | 2   | 2          | 2   | ns   |

$\dagger$  This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

**switching characteristics over recommended operating free-air temperature range,**  
 **$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT)              | TO (OUTPUT)   | LOAD CAPACITANCE     | $T_A = 25^\circ\text{C}$ |      |       | SN54AHC595 |       | SN74AHC595 |      | UNIT |
|-----------|---------------------------|---------------|----------------------|--------------------------|------|-------|------------|-------|------------|------|------|
|           |                           |               |                      | MIN                      | TYP  | MAX   | MIN        | MAX   | MIN        | MAX  |      |
| $f_{max}$ |                           |               | $C_L = 15\text{ pF}$ | 80*                      | 120* |       | 70*        |       | 70         |      | MHz  |
|           |                           |               | $C_L = 50\text{ pF}$ | 55                       | 105  |       | 50         |       | 50         |      |      |
| $t_{PLH}$ | RCLK                      | $Q_A$ - $Q_H$ | $C_L = 15\text{ pF}$ |                          | 6*   | 11.9* | 1*         | 13.5* | 1          | 13.5 | ns   |
| $t_{PHL}$ |                           |               |                      |                          | 6*   | 11.9* | 1*         | 13.5* | 1          | 13.5 |      |
| $t_{PLH}$ | SRCLK                     | $Q_H'$        | $C_L = 15\text{ pF}$ |                          | 6.6* | 13*   | 1*         | 15*   | 1          | 15   | ns   |
| $t_{PHL}$ |                           |               |                      |                          | 6.6* | 13*   | 1*         | 15*   | 1          | 15   |      |
| $t_{PHL}$ | $\overline{\text{SRCLR}}$ | $Q_H'$        | $C_L = 15\text{ pF}$ |                          | 6.2* | 12.8* | 1*         | 13.7* | 1          | 13.7 | ns   |
| $t_{PZH}$ | $\overline{\text{OE}}$    | $Q_A$ - $Q_H$ | $C_L = 15\text{ pF}$ |                          | 6*   | 11.5* | 1*         | 13.5* | 1          | 13.5 | ns   |
| $t_{PZL}$ |                           |               |                      |                          | 7.8* | 11.5* | 1*         | 13.5* | 1          | 13.5 |      |
| $t_{PLH}$ | RCLK                      | $Q_A$ - $Q_H$ | $C_L = 50\text{ pF}$ |                          | 7.9  | 15.4  | 1          | 17    | 1          | 17   | ns   |
| $t_{PHL}$ |                           |               |                      |                          | 7.9  | 15.4  | 1          | 17    | 1          | 17   |      |
| $t_{PLH}$ | SRCLK                     | $Q_H'$        | $C_L = 50\text{ pF}$ |                          | 9.2  | 16.5  | 1          | 18.5  | 1          | 18.5 | ns   |
| $t_{PHL}$ |                           |               |                      |                          | 9.2  | 16.5  | 1          | 18.5  | 1          | 18.5 |      |
| $t_{PHL}$ | $\overline{\text{SRCLR}}$ | $Q_H'$        | $C_L = 50\text{ pF}$ |                          | 9    | 16.3  | 1          | 17.2  | 1          | 17.2 | ns   |
| $t_{PZH}$ | $\overline{\text{OE}}$    | $Q_A$ - $Q_H$ | $C_L = 50\text{ pF}$ |                          | 7.8  | 15    | 1          | 17    | 1          | 17   | ns   |
| $t_{PZL}$ |                           |               |                      |                          | 9.6  | 15    | 1          | 17    | 1          | 17   |      |
| $t_{PHZ}$ | $\overline{\text{OE}}$    | $Q_A$ - $Q_H$ | $C_L = 50\text{ pF}$ |                          | 8.1  | 15.7  | 1          | 16.2  | 1          | 16.2 | ns   |
| $t_{PLZ}$ |                           |               |                      |                          | 9.3  | 15.7  | 1          | 16.2  | 1          | 16.2 |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

# SN54AHC595, SN74AHC595

## 8-BIT SHIFT REGISTERS

### WITH 3-STATE OUTPUT REGISTERS

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)           | TO<br>(OUTPUT) | LOAD<br>CAPACITANCE  | $T_A = 25^\circ\text{C}$ |      |      | SN54AHC595 |      | SN74AHC595 |      | UNIT |
|------------------|---------------------------|----------------|----------------------|--------------------------|------|------|------------|------|------------|------|------|
|                  |                           |                |                      | MIN                      | TYP  | MAX  | MIN        | MAX  | MIN        | MAX  |      |
| $f_{\text{max}}$ |                           |                | $C_L = 15\text{ pF}$ | 135*                     | 170* |      | 115*       |      | 115        |      | MHz  |
|                  |                           |                | $C_L = 50\text{ pF}$ | 95                       | 140  |      | 85         |      | 85         |      |      |
| $t_{\text{PLH}}$ | RCLK                      | $Q_A-Q_H$      | $C_L = 15\text{ pF}$ |                          | 4.3* | 7.4* | 1*         | 8.5* | 1          | 8.5  | ns   |
| $t_{\text{PHL}}$ |                           |                |                      |                          | 4.3* | 7.4* | 1*         | 8.5* | 1          | 8.5  |      |
| $t_{\text{PLH}}$ | SRCLK                     | $Q_{H'}$       | $C_L = 15\text{ pF}$ |                          | 4.5* | 8.2* | 1*         | 9.4* | 1          | 9.4  | ns   |
| $t_{\text{PHL}}$ |                           |                |                      |                          | 4.5* | 8.2* | 1*         | 9.4* | 1          | 9.4  |      |
| $t_{\text{PHL}}$ | $\overline{\text{SRCLR}}$ | $Q_{H'}$       | $C_L = 15\text{ pF}$ |                          | 4.5* | 8*   | 1*         | 9.1* | 1          | 9.1  | ns   |
| $t_{\text{PZH}}$ | $\overline{\text{OE}}$    | $Q_A-Q_H$      | $C_L = 15\text{ pF}$ |                          | 4.3* | 8.6* | 1*         | 10*  | 1          | 10   | ns   |
| $t_{\text{PZL}}$ |                           |                |                      |                          | 5.4* | 8.6* | 1*         | 10*  | 1          | 10   |      |
| $t_{\text{PLH}}$ | RCLK                      | $Q_A-Q_H$      | $C_L = 50\text{ pF}$ |                          | 5.6  | 9.4  | 1          | 10.5 | 1          | 10.5 | ns   |
| $t_{\text{PHL}}$ |                           |                |                      |                          | 5.6  | 9.4  | 1          | 10.5 | 1          | 10.5 |      |
| $t_{\text{PLH}}$ | SRCLK                     | $Q_{H'}$       | $C_L = 50\text{ pF}$ |                          | 6.4  | 10.2 | 1          | 11.4 | 1          | 11.4 | ns   |
| $t_{\text{PHL}}$ |                           |                |                      |                          | 6.4  | 10.2 | 1          | 11.4 | 1          | 11.4 |      |
| $t_{\text{PHL}}$ | $\overline{\text{SRCLR}}$ | $Q_{H'}$       | $C_L = 50\text{ pF}$ |                          | 6.4  | 10   | 1          | 11.1 | 1          | 11.1 | ns   |
| $t_{\text{PZH}}$ | $\overline{\text{OE}}$    | $Q_A-Q_H$      | $C_L = 50\text{ pF}$ |                          | 5.7  | 10.6 | 1          | 12   | 1          | 12   | ns   |
| $t_{\text{PZL}}$ |                           |                |                      |                          | 6.8  | 10.6 | 1          | 12   | 1          | 12   |      |
| $t_{\text{PHZ}}$ | $\overline{\text{OE}}$    | $Q_A-Q_H$      | $C_L = 50\text{ pF}$ |                          | 3.5  | 10.3 | 1          | 11   | 1          | 11   | ns   |
| $t_{\text{PLZ}}$ |                           |                |                      |                          | 3.4  | 10.3 | 1          | 11   | 1          | 11   |      |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

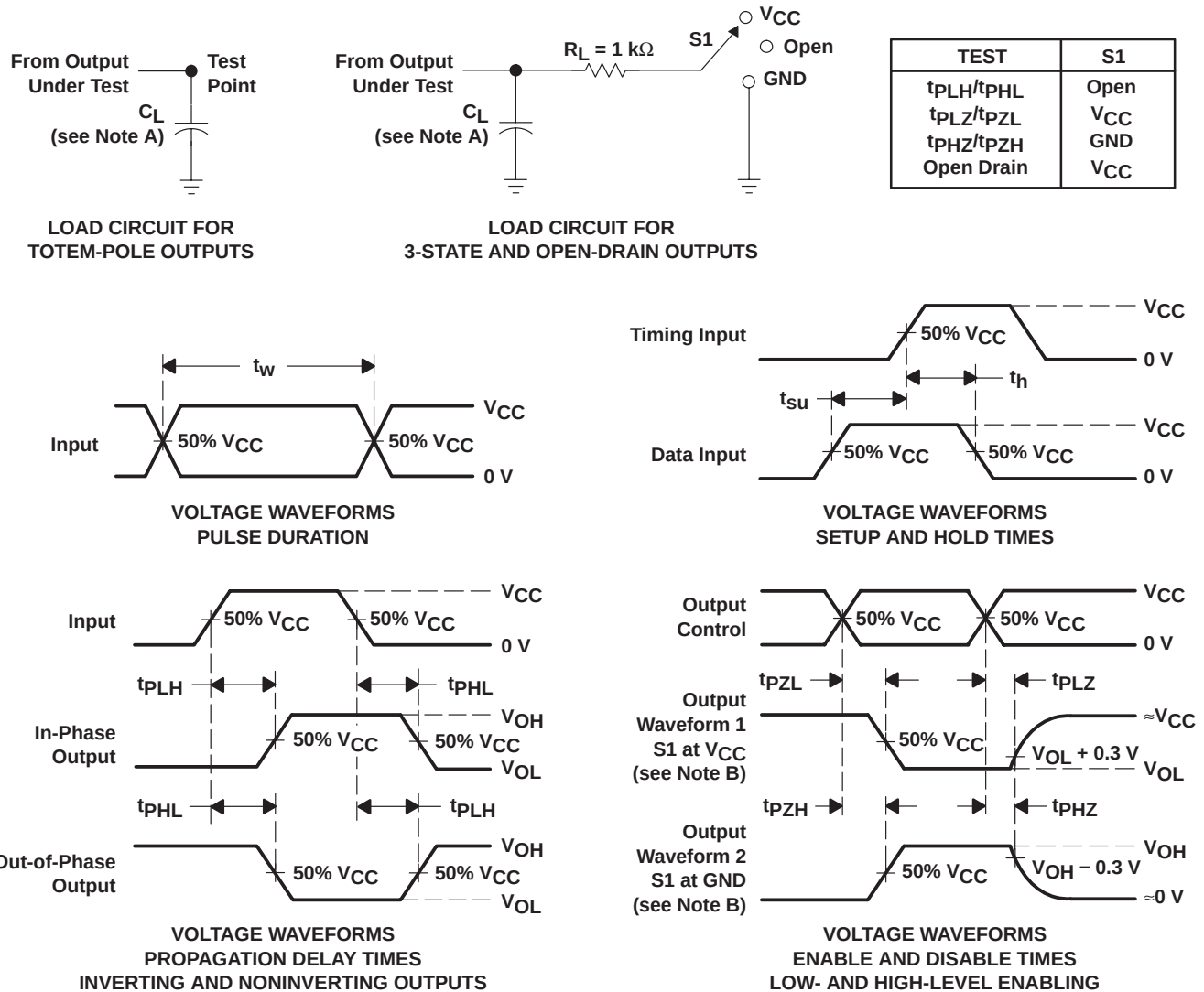
operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER                                     | TEST CONDITIONS             | TYP  | UNIT |
|-----------------------------------------------|-----------------------------|------|------|
| $C_{\text{pd}}$ Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 25.2 | pF   |

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AHC595D      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DBR    | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DBRE4  | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DBRG4  | ACTIVE                | SSOP         | DB              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DE4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DG4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DR     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DRE4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595DRG4   | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595N      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74AHC595NE4    | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74AHC595NSR    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595NSRE4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595NSRG4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595PW     | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595PWE4   | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595PWG4   | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595PWR    | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595PWRE4  | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AHC595PWRG4  | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

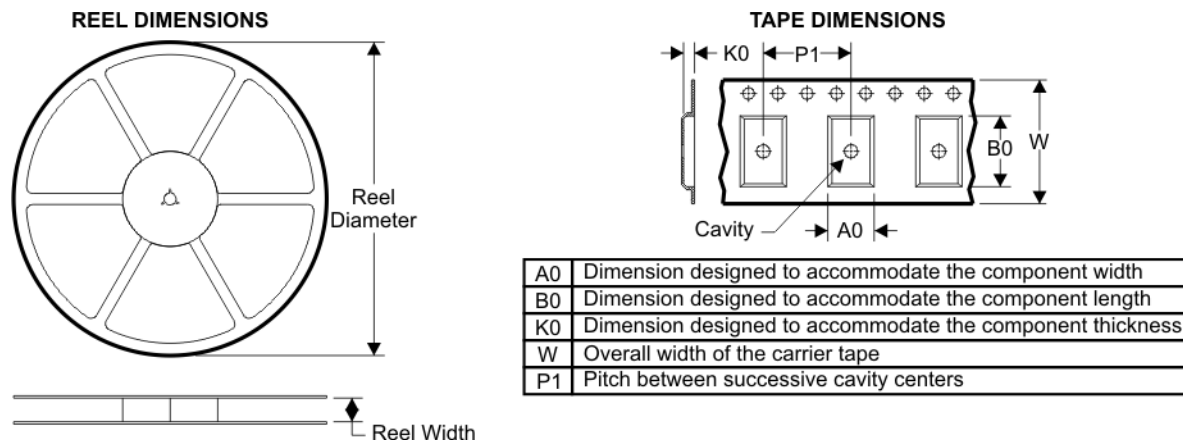
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

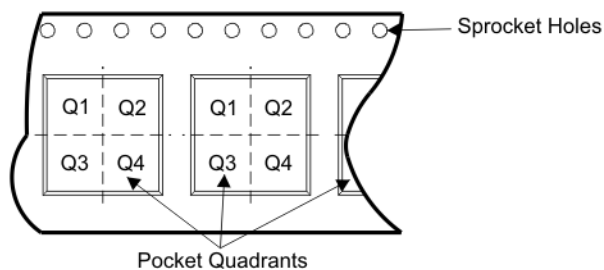
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**TAPE AND REEL BOX INFORMATION**

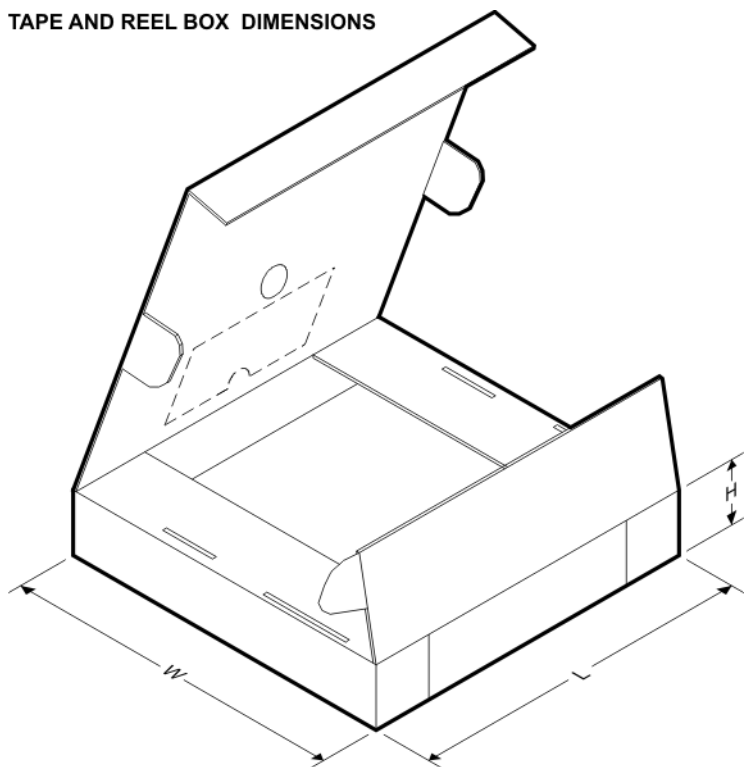


**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



| Device        | Package | Pins | Site    | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|---------|------|---------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC595DBR | DB      | 16   | SITE 41 | 330                | 16              | 8.2     | 6.6     | 2.5     | 12      | 16     | Q1            |
| SN74AHC595DR  | D       | 16   | SITE 27 | 330                | 16              | 6.5     | 10.3    | 2.1     | 8       | 16     | Q1            |
| SN74AHC595DR  | D       | 16   | SITE 41 | 330                | 16              | 6.5     | 10.3    | 2.1     | 8       | 16     | Q1            |
| SN74AHC595NSR | NS      | 16   | SITE 41 | 330                | 16              | 8.2     | 10.5    | 2.5     | 12      | 16     | Q1            |
| SN74AHC595PWR | PW      | 16   | SITE 41 | 330                | 12              | 7.0     | 5.6     | 1.6     | 8       | 12     | Q1            |

## TAPE AND REEL BOX DIMENSIONS

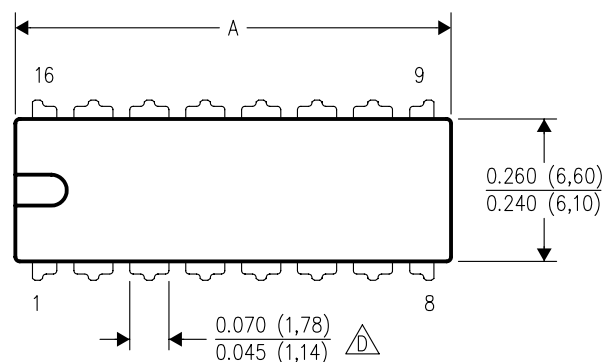


| Device        | Package | Pins | Site    | Length (mm) | Width (mm) | Height (mm) |
|---------------|---------|------|---------|-------------|------------|-------------|
| SN74AHC595DBR | DB      | 16   | SITE 41 | 346.0       | 346.0      | 33.0        |
| SN74AHC595DR  | D       | 16   | SITE 27 | 342.9       | 336.6      | 28.58       |
| SN74AHC595DR  | D       | 16   | SITE 41 | 346.0       | 346.0      | 33.0        |
| SN74AHC595NSR | NS      | 16   | SITE 41 | 346.0       | 346.0      | 33.0        |
| SN74AHC595PWR | PW      | 16   | SITE 41 | 346.0       | 346.0      | 29.0        |

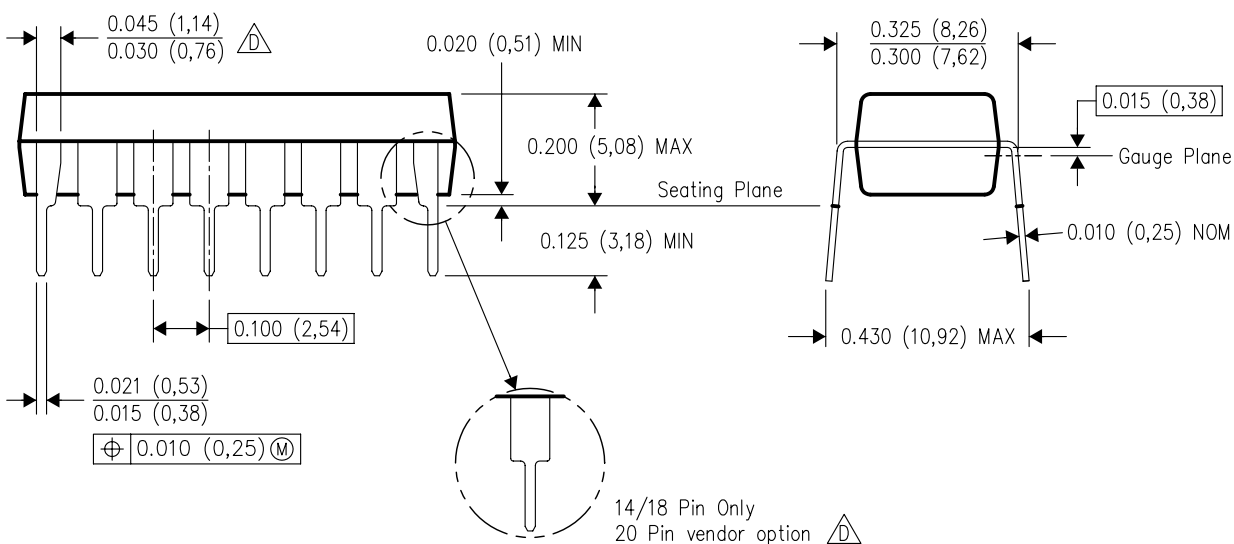
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



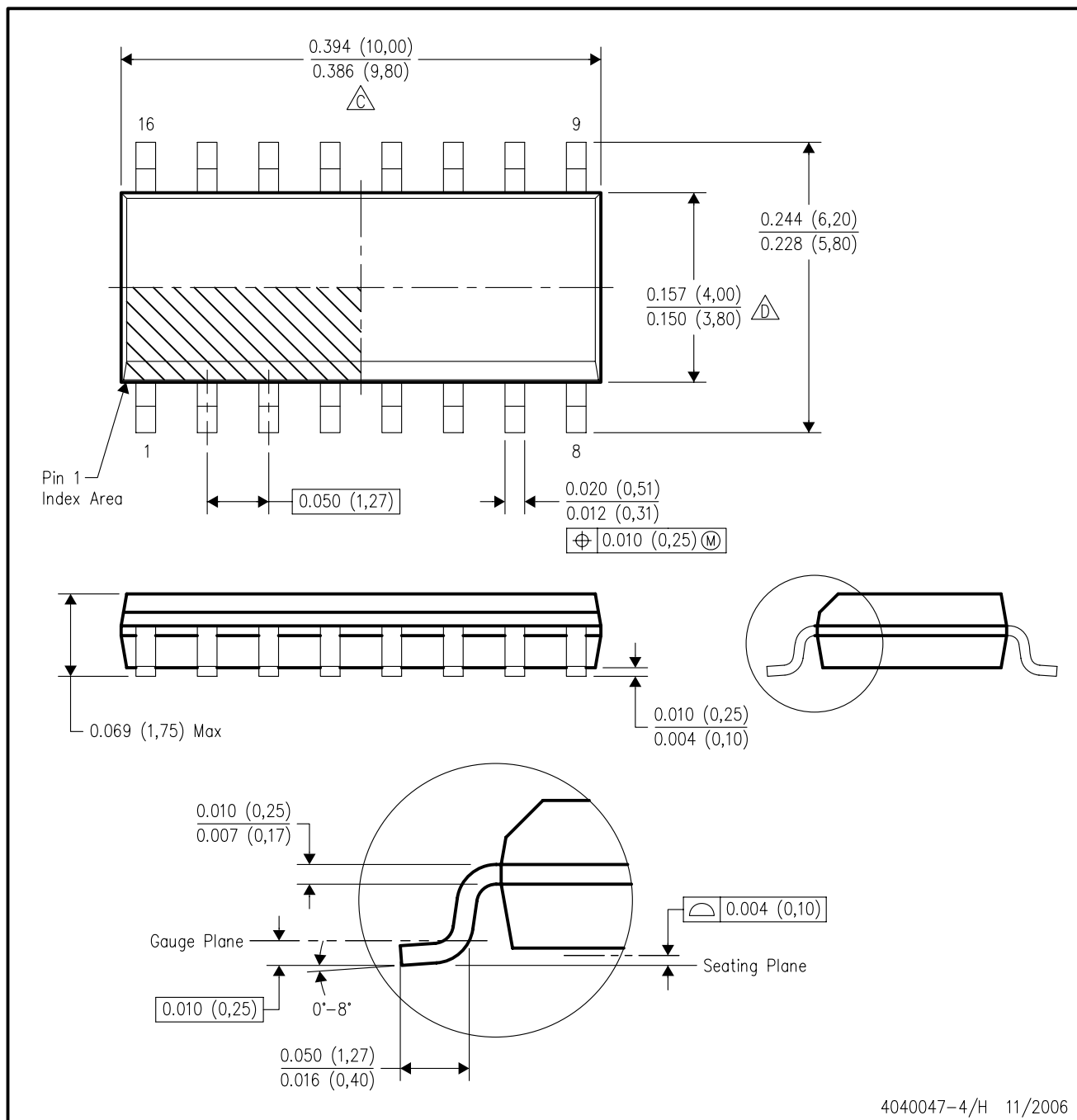
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

## NOTES:

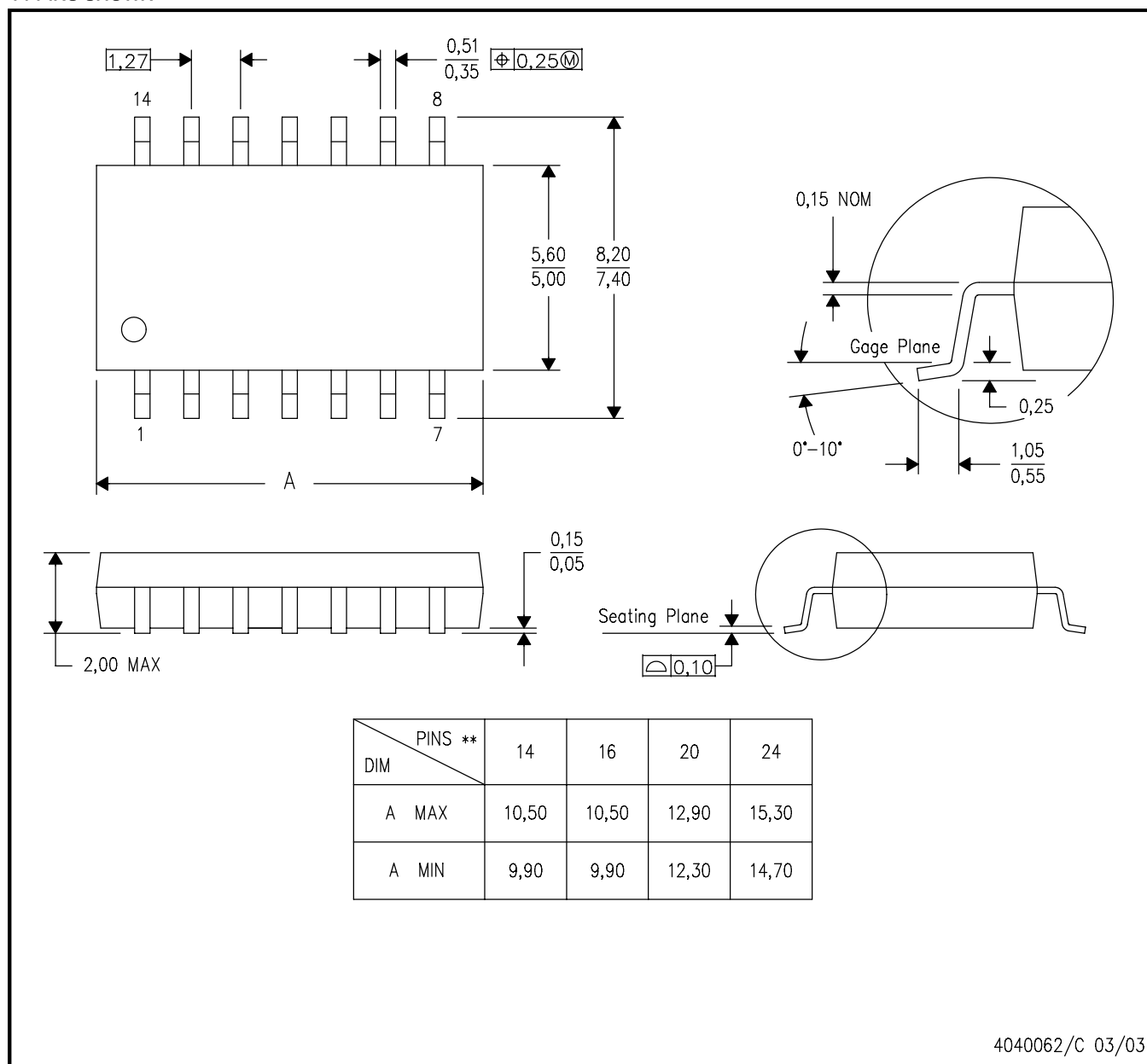
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

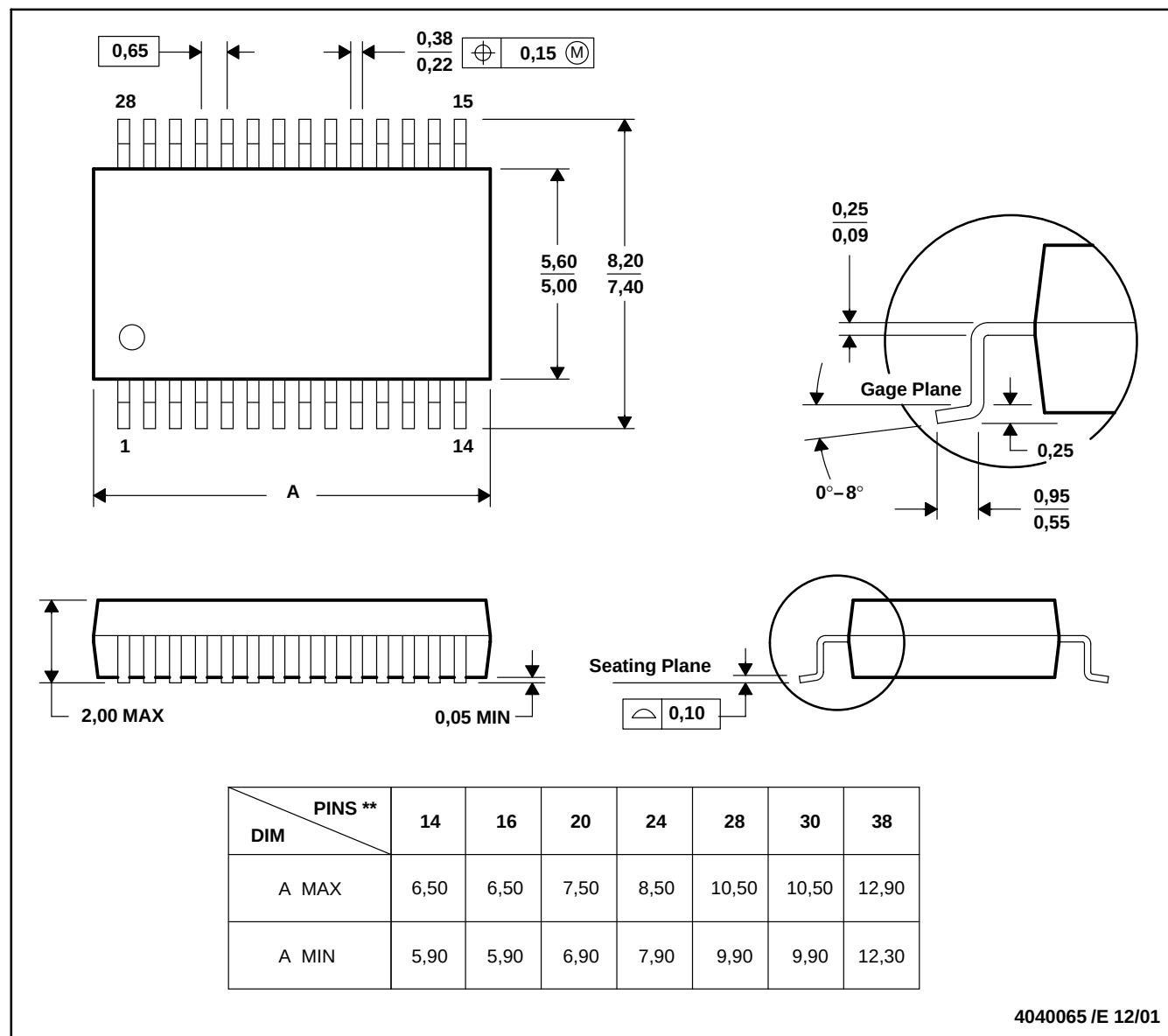


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

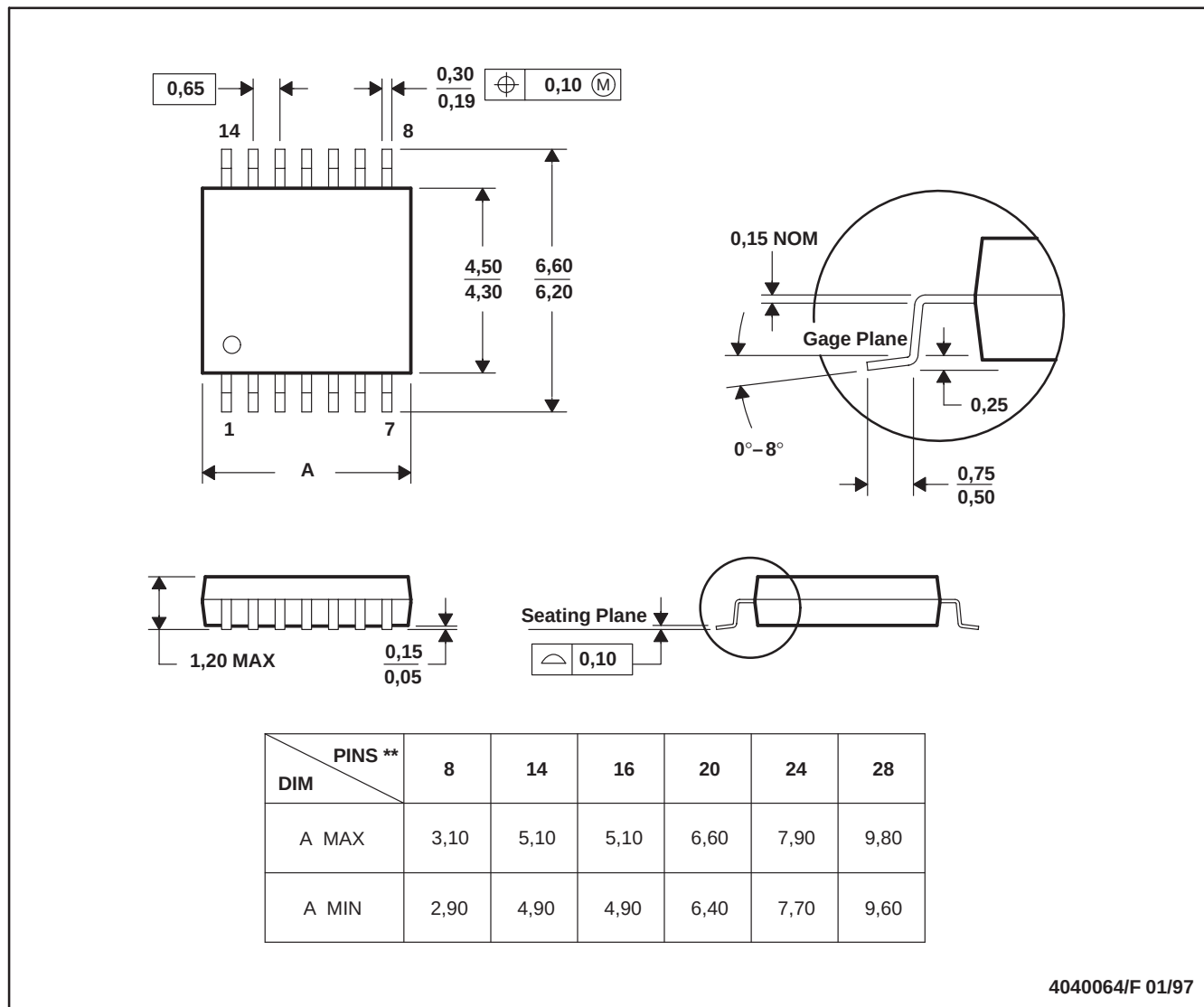


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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